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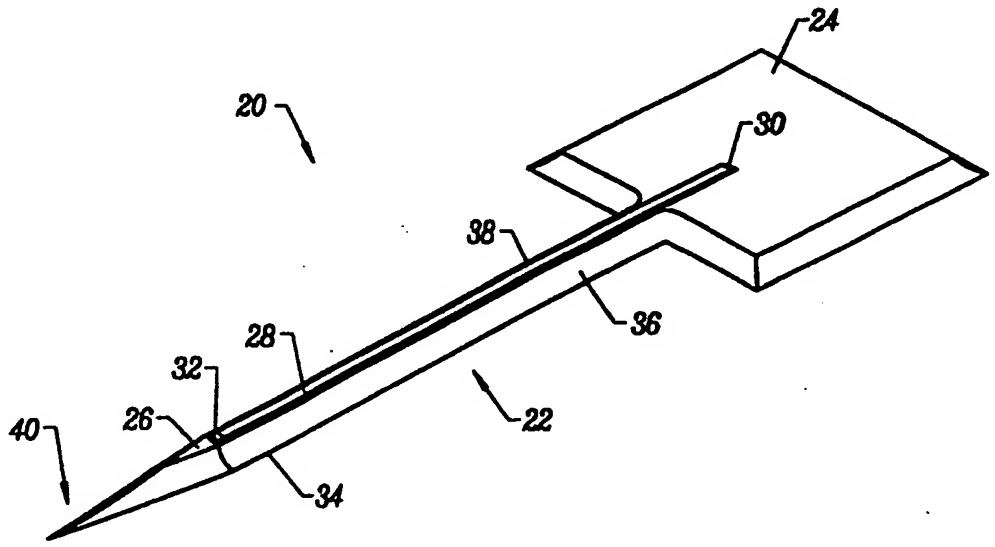

(57) Abstract

A probe (20) includes an elongated body (22) with a top surface (26), a bottom surface (34), a frist sidewall (36) between the top surface (26) and the bottom surface (34), and a second sidewall (38) between the top surface (26) and the bottom surface (34). An end (40) is defined by the bottom surface (34) converging into a tip, an isotropic etched portion of the frist sidewall (36) converging into the tip (34), and an isotropic etched portion of the second wall (38) converting into the tip (34). The elongated body is less than approximately 700 micrometers wide, and less than approximately 200 micrometers thick. The elongated body may incorporate a fluid channel. The elongated body may be formed of silicon that is not doped with boron

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TRANSDERMAL PROBE WITH AN ISOTROPICALLY ETCHED TIP, AND METHOD OF FABRICATING SUCH A DEVICE

Brief Description of the Invention

This invention relates generally to micron-scale transdermal probes, such as hypodermic needles, lancets, and blades. More particularly, this invention relates to a micron-scale transdermal probe that is formed by isotropic etching of a single crystal substrate.

Background of the Invention

The biomedical industry seeks to replace stainless steel hypodermic injection needles with needles that have small diameters, sharper tips, and which can provide additional functionality. The advantages of smaller diameters and sharper tips are to minimize pain and tissue damage. Desirable additional functionality for a hypodermic injection needle includes the capability of providing integrated electronics for chemical concentration monitoring, cell stimulation, and the control of fluid flow, such as through an integrated valve or pump.

Integrated circuit technology and single crystal silicon wafers have been used to produce hypodermic injection needles. A "microhypodermic" injection needle or "microneedle" is described in Lin, et al., "Silicon Processed Microneedle", *Digest of Transducers '93, International Conference on Solid-State Sensors and Actuators*, pp. 237-240, June 1993. Another microneedle is described in Chen and Wise, "A Multichannel Neural Probe for Selective Chemical Delivery at the Cellular Level," *Technical Digest of the Solid-State Sensor and Actuator Workshop*, Hilton head

Island, S.C., pp. 256-259, June 13-16, 1994. The needles described in these references have common elements since they are both based on the process flow for a multielectrode probe. In particular, both processes rely on heavily boron doped regions to define the shape of the needle and the utilization of ethylenediamine pyrocatechol as an anisotropic etchant.

Lin, et al. describe a fluid passage that is surface micromachined and utilizes a timed etch to thin the wafer such that an approximately 50 μm thick strengthening rib of single crystal silicon remains. In contrast, Chen and Wise bulk micromachine a channel into the microneedle using an anisotropic etch and all of the single crystal silicon comprising the shaft of the needle is heavily boron doped so the timing of the anisotropic etch to form the shape of the needle is less critical.

There are a number of disadvantages associated with these prior art devices. The single crystal silicon strengthening rib in the Lin, et al. microneedle is naturally rough and is difficult to reproduce due to the tight tolerance on the timed etch. The Chen and Wise microneedle results in walls approximately 10 μm or less in thickness and the shape of the fluid channel defines the shape of the silicon comprising the structural portion of the needle. Therefore, small channels lead to thin needles and large channels lead to large needles. This is a problem when a needle with a small channel but large needle cross-section is desired. Often, large needle cross-sections are necessary, such as those 50 μm thick or greater, to obtain a stronger microneedle, but since the fluid flow rate is dependent on the cross-section of the needle, a large needle may not provide the necessary flow resistance. To establish the necessary flow resistance in a large needle cross-section, a complicated nested channel configuration must be fabricated.

The Lin, et al. and Chen and Wise microneedles share the drawback that they rely on the use of boron doping to define the shape of the needle. This requires a long (approximately 8 hours in Chen and Wise; approximately 16 hours in Lin), high temperature (approximately 1150°C) step which is expensive. In addition, the chosen anisotropic etchant is ethylenediamine pyrocatechol, which is a strong carcinogen, making production dangerous and therefore leading to further expenses. Finally, since both of these microneedles utilize an anisotropic etchant to produce the shape of the microneedle, limitations are placed on the geometry of the needle. For the needle to be "sharpest", it is preferred for the tip of the needle to originate from a near

infinitesimally small point and taper continuously, without step transitions, to the full width of the shaft of the needle. Such a geometry is not possible using the techniques described in Lin, et al. and Chen and Wise. In particular, the needles produced using those techniques have abrupt step transitions, largely attributable to the use of the anisotropic etchant.

Microneedles that do not include a channel are referred to herein as lancets. Lancets may be used to lance the epidermis so that a drop of blood can be sampled. Lancets may also be formed in configurations that allow them be used as blades or scalpals. Such devices can be used for cutting skin or eyes in a surgical context. Thus, as used herein, a transdermal probe refers to microneedles, lancets, or blades (scalpals).

It would be highly desirable to provide improved transdermal probes and processes of fabricating such probes to overcome the shortcomings associated with prior art devices.

Summary of the Invention

A transdermal probe includes an elongated body with a top surface, a bottom surface, a first side wall between the top surface and the bottom surface, and a second side wall between the top surface and the bottom surface. An end is defined by the bottom surface converging into a tip, an isotropically etched portion of the first side wall converging into the tip, and an isotropically etched portion of the second side wall converging into the tip. The elongated body is less than approximately 700μm wide and less than approximately 200μm thick. The elongated body may incorporate a fluid channel. The elongated body may be formed of silicon that is not doped with Boron. In such a configuration, integrated circuitry or a micromachined device, such as a heater or pump may also be formed on the device. A number of novel processing techniques are associated with the fabrication of the device. The device may be formed by relying solely on isotropic etching. Alternately, a combination of isotropic and anisotropic etching may be used. Unlike prior art micromachined devices, the disclosed device may be processed at relatively low temperatures of 1100°C or below and without using the carcinogen ethylenediamin pyrocatechol. When forming a blade, the width can be as wide as about 3 mm and the thickness can be as high as about 400 μm.

Brief Description of the Drawings

For a better understanding of the nature and objects of the invention, reference should be made to the following detailed description taken in conjunction with the accompanying drawings, in which:

FIG. 1 is a perspective view of an isotropically etched probe in accordance with an embodiment of the invention.

FIG. 2 is an enlarged view of the tip of the probe shown in Fig. 1.

FIG. 3 is a top view of the probe shown in Fig. 1.

FIG. 4 is a side view of the probe shown in Fig. 1.

FIG. 5 is a front view of the probe shown in Fig. 1.

FIG. 6 is a perspective view of an isotropically and anisotropically etched probe in accordance with an embodiment of the invention.

FIG. 7 is an enlarged view of the tip of the probe shown in Fig. 6.

FIGS. 8a-8e illustrate different etched channels in accordance with embodiments of the invention.

FIGS. 9a-9e illustrate the construction of a probe in accordance with a first example of the invention.

FIGS. 10a-10i illustrate the construction of a probe in accordance with a second example of the invention.

FIGS. 11a-11L illustrate the construction of a probe in accordance with a third example of the invention.

FIGS. 12a-12L illustrate the construction of a probe in accordance with a fourth example of the invention.

FIGS. 13a-13q' illustrate the construction of a probe in accordance with a fifth example of the invention.

FIGS. 14a-14m' illustrate the construction of a probe in accordance with a sixth example of the invention.

FIGS. 15a-15m' illustrate the construction of a probe in accordance with a seventh example of the invention.

FIGS. 16a-16o' illustrate the construction of a probe in accordance with an eighth example of the invention.

FIGS. 17a-17f illustrates the construction of a probe in accordance with a ninth example of the invention.

FIGS. 18a-18h illustrate the construction of a probe in accordance with a tenth example of the invention.

FIGS. 19a-19i illustrate the construction of a probe in accordance with an eleventh example of the invention.

FIGS. 20a-20f illustrates the construction of a probe in accordance with a twelfth example of the invention.

FIG. 21 illustrates isotropic etchant etch rate of PSG deposited using various phosphine flow rate parameters in accordance with the invention.

FIGS. 22A and 22B are perspective views of lancets constructed in accordance with the invention.

FIG. 23 illustrates an abrader constructed in accordance with an embodiment of the invention.

FIG. 24 is an enlarged view of isotropically etched tips associated with the abrader of FIG. 23.

FIG. 25a-e illustrates the construction of an abrader with sharp tips in accordance with a thirteenth example of the invention.

FIG. 26a-e illustrates the construction of an abrader with flat tips in accordance with a fourteenth example of the invention.

FIG. 27a-e illustrates the construction of an abrader with pyramidal projections in accordance with a fifteenth example of the invention.

Like reference numerals refer to corresponding parts throughout the several views of the drawings.

Detailed Description of the Invention

Fig. 1 provides a perspective view of an isotropically etched transdermal probe 20 in accordance with an embodiment of the invention. The probe 20 includes an elongated body 22, formed of single crystal material, preferably silicon, which terminates in a shank end 24. The elongated body 22 has a top, preferably horizontal, surface 26. In the embodiment of Fig. 1, the top surface 26 has a channel cap 28, including a channel inlet/outlet port 30 and a channel outlet/inlet port 32. As will be shown below, embodiments of the probe of the invention include an integrally formed channel within the elongated body 22. The channel cap 28, which may be formed with polycrystalline silicon, covers the channel. The channel cap inlet port 30 allows fluid

to enter the channel and the channel cap outlet port 32 allows fluid to exit the channel. In this configuration, the probe 20 of the invention can be used to deliver or draw fluid from a vessel, such as a living body or a drug container. Embodiments of the probe 20 do not include a channel, such embodiments are useful as lancets, which are used to lance human tissue for the purpose of drawing blood. In other embodiments of the invention, the probe may be used as a blade.

The elongated body 22 also includes a bottom, preferably horizontal, surface 34. Connected between the top surface 26 and bottom surface 34 is a first side wall 36 and a second side wall 38. In the embodiment of Fig. 1, each side wall has a curved shape attributable to an isotropic etch operation, discussed below.

Fig. 2 is an enlarged view of the distal end or tip 40 of the elongated body 22. The figure illustrates the top surface 26, the channel cap 28, the channel cap outlet port 32, the bottom surface 34, the first side wall 36, and the second side wall 38. Observe that the bottom surface 34 converges into the tip 40. In particular, the bottom horizontal surface 34 horizontally converges into the tip 40. Since isotropic etching techniques are used, the tip 40 can be near infinitesimally small.

Fig. 2 also illustrates that the first side wall 36 converges into the tip 40, as does the second side wall 38. In particular, each side wall 36 and 38 horizontally and vertically converges into the tip 40 in a smooth manner, without any step transitions. The first side wall 36 and the second side wall 38 meet one another to form a rib 42, which smoothly extends into the tip 40.

The tip 40 formed in accordance with the present invention is sharper than prior art probes because the processing to form the tip allows for a tip which originates from a nearly infinitesimal point that tapers to the full dimensions of the elongated body 22.

Fig. 3 is a top view of the isotropically etched probe 20. The figure clearly shows the previously described elements, including the shank end 24, the top surface 26, the channel cap 28, the channel cap inlet port 30, the channel cap outlet port 32, the first side wall 36, the second side wall 38, and the tip 40.

Fig. 4 is a side view of the probe 20. The figure shows the shank end 24, the top surface 26, the channel cap 28, the bottom surface 34, the first side wall 36, and the tip 40. Observe the curved surface leading to the tip 40. This smooth surface, without abrupt step transitions is attributable to the isotropic etching operation used in accordance with the invention.

Fig. 5 is a front view of the probe 20. The figure shows the shank end 24, the top surface 26, the channel cap 28, the bottom surface 34. The figure also shows curved side walls 36 and 38. The curved sidewalls avoid abrupt step transitions associated with prior art probes. The curved sidewalls are attributable to the isotropic etching operation of the invention.

Fig. 6 is a perspective view of an isotropically/anisotropically etched probe 50 in accordance with another embodiment of the invention. The probe 50 includes an elongated body 52 which terminates in a shank end 54. The device includes a top horizontal surface 56, which supports a channel cap 58. The channel cap 58 includes a channel cap inlet port 60 and a channel cap outlet port 62. Fig. 6 also shows a first vertical side wall 66, positioned between the top horizontal surface 56 and a bottom horizontal surface 64. A second vertical side wall (not shown) exists on the other side of the device.

Fig. 7 is an enlarged perspective view of the distal end or tip 70 of the elongated body 52. Fig. 7 clearly shows the vertical side wall 66, which stands in contrast to the curved sidewalls of the device of Figs. 1-5. The tip 70 is formed using a combination of isotropic and anisotropic etching. The anisotropic etching provides the vertical side walls, while the isotropic etching provides the smooth transition into the tip 70. The tip has smooth surfaces and otherwise avoids abrupt step transitions between the tip 70 and the cross-sectional area of the elongated body 52.

Figs. 8a-8e illustrate different isotropically and anisotropically etched channels in accordance with different embodiments of the invention. Fig. 8a illustrates an isotropically etched probe 20 with isotropically etched sidewalls 36 and 38. The figure also shows a polysilicon shell 28. Fig. 8b is a similar figure, but shows a channel 72 formed with an anisotropic etch of a (100) silicon wafer. Fig. 8c shows a channel 73 formed with an isotropic etch. Fig. 8d shows a channel 74 isotropically etched with a flat bottom. Finally, Fig. 8e shows a channel 76 which is vertically etched.

As will be demonstrated below, the invention can be implemented using a wide variety of processing techniques. The examples provided herein are for the purpose of illustration. The invention should in no way be construed to be limited to the described examples.

Not only have a large number of processing techniques been used to implement the invention, but a variety of devices sizes have also been used. By way of example, the devices of Figs. 8a-8e were implemented as 300 μm wide and 100 μm thick devices. The elongated body 52 of Fig. 6 has been implemented as a 100 μm square cross-sectional device. A vertically etched trench formed through a double sided alignment and etching technique has resulted in 290 μm wide and 100 μm thick devices. Double sided alignment and etching on a standard thickness (500 μm) wafer has produced devices that are 640 μm wide and 120 μm thick. In general, the invention is implemented with an elongated body that is less than approximately 700 μm wide and less than approximately 200 μm thick. More preferably, the invention is implemented with an elongated body that is less than approximately 300 μm wide and less than approximately 150 μm thick. In the case of a blade, the width of the blade can be approximately 3 mm, and its thickness can be as high as 400 μm.

Advantageously, many of the processing techniques described below use silicon-on-insulator (SOI) wafers. The fabrication of probes using SOI wafers greatly simplifies processing. The type of SOI wafers typically used to fabricate the probes described in the application are comprised of two silicon wafers that are bonded together through an intermediate insulator material, typically silicon dioxide. The top wafer (device wafer) is thinned to the desired thickness of the probe using a combination of grinding and polishing techniques. The role of the bottom wafer (handle wafer) is to provide a strong substrate for easy handling. Since the fabrication of the probe is done solely on the device layer, the purpose of the insulator material is to provide an etch stop to prevent etching into the handle layer.

Suppliers are able to provide SOI wafers with a specified overall thickness, a specified device layer thickness, and a specified thickness of insulating layer. The availability of SOI wafers permits the use of standard integrated circuit processing equipment since the overall thickness of the wafer is the same as a standard wafer. Also, the thickness of the needles can be better controlled since SOI wafer suppliers are able to guarantee a device layer thickness to within a few micrometers and this thickness is known before processing. Additionally, no wafer thinning steps, which are a common cause of probe thickness variations, beyond those of the SOI wafer supplier are required and no boron doping and EDP is required to define the probe

shape. Finally, since the insulating layer provides an etch stop, the timing of the etch is not critical.

The following processing steps have been used, as described below, to construct a variety of devices, in accordance with the invention. Those skilled in the art will appreciate that a variety of modifications on the specified steps are feasible, yet still within the scope of the invention.

TABLE 1 – PREFERRED FABRICATION STEPS

A. STANDARD WAFER CLEANING

Use VLSI lab sink
Piranha clean (H_2SO_4:H_2O_2, 5:1) for 10 minutes
Two, one minute rinses in de-ionized (DI) water
Rinse until resistivity of water is > 11 MΩ-cm
Spin dry

Piranha clean (H_2SO_4:H_2O_2, 5:1) for 10 minutes at 120°C
Rinse in DI water for one minute
Dip in 25:1 HF until hydrophobic
Two, one minute rinses in DI water
Rinse until resistivity of DI water is > 14 MΩ-cm
Spin Dry

B. CLEAN WAFERS WITH MINIMAL OXIDE STRIP

Use VLSI lab sink
Piranha clean (H_2SO_4:H_2O_2, 5:1) for 10 minutes
Rinse in DI water for one minute
Dip in 25:1 HF briefly until native silicon oxide is removed
Two, one minute rinses in DI water
Rinse until resistivity of DI water is > 14 MΩ-cm
Spin Dry

C. PARTIALLY CLEAN WAFERS

Use VLSI lab sink

Piranha clean (H_2SO_4:H_2O_2, 5:1) for 10 minutes

Two, one minute rinses in DI water

Rinse until resistivity of DI water is > 11 MΩ-cm

Spin Dry

D. DEPOSIT LOW-STRESS SILICON NITRIDE

Use a horizontal low pressure chemical vapor deposition reactor

Target thickness as specified

Conditions = 835°C, 140 mTorr, 100 sccm DCS, and 25 sccm NH_3

E. DEPOSIT PHOSPHOSILICATE GLASS (PSG)

Use a horizontal low pressure chemical vapor deposition reactor

Target thickness as specified

Conditions = 450°C, 300 mTorr, 60 sccm SiH_4, 90 sccm 0_2 and 5.2 sccm PH_3

G. DENSIFY LPCVD OXIDE

F. DEPOSIT LOW TEMPERATURE OXIDE (LTO)

Use a horizontal low pressure chemical vapor deposition reactor

Target thickness as specified

Conditions = 450°C, 300 mTorr, 60 sccm SiH_4, and 90 sccm 0_2

G. DENSIFY LPCVD OXIDE

G. DENSIFY LPCVD OXIDE

Use horizontal atmospheric pressure reactor

Conditions = 950°C, N_2, 1 hour; alternately, 1100°C with a stream environment rather than N_2

H. PHOTOLITHOGRAPHY

1. HMDS prime

2. Photoresist coat: Coat 1 μm of Shipley S3813 (thickness may need to be varied depending on topography and thickness of material to be etched) multi-wavelength positive resist

3. Expose resist: G-line wafer stepper, standard exposure time

4. Resist develop: Standard develop using Shipley MF319

5. Hard bake for 30 minutes

I. COAT BACKSIDE WITH PHOTORESIST

1. HMDS prime

2. Photoresist coat: Coat 1 μm of Shipley S3813 (thickness may need to be varied depending on topography and thickness of material to be etched) multi-wavelength positive resist

3. Resist develop: Standard develop using Shipley MF 319

4. Hard bake for 30 minutes

J. OXIDE WET ETCHING

Use VLSI lab sink

Etch in 5:1 BHF until desired amount of oxide has been removed

Two, one minute rinses in DI water

Rinse until resistivity of water is > 11 MΩ-cm

Spin dry

K. RESIST STRIP

Use lab sink

PRS-2000, heated to 90°C, 10 minutes

Rinse in three baths of DI water, 2 minutes each

C. PARTIAL CLEAN WAFERS

L. NITRIDE ETCH

SF_6+He plasma etch

Etch until desired amount of nitride has been removed

M. DEPOSIT UNDOPED POLYSILICON

Use horizontal low pressure chemical vapor deposition reactor

Target thickness as specified

Conditions = 605°C, 555 mTorr, and 125 sccm SiH_4; alternately, 580°C, 300 mTorr, and 100 sccm SiH_4

N. POLYSILICON ETCH

Chlorine plasma etch

Etch until desired amount of polysilicon has been removed

O. ISOTROPIC SILICON ETCH

Use lab sink

Submerge in silicon etchant (64% HNO_3/ 33%H_2O/ 3% NH_4F) until desired amount of silicon has been removed

Rinse in DI water for 1 hour

(Various concentrations of NH_4F will work. In addition, there are many isotropic etches involving HF, HNO_3, and $C_2H_4O_2$ and etches involving HF, HNO_3, XeF_2, SF_6 and H_2O that may be used in connection with the invention.)

P. ANISOTROPIC WET ETCH

Use lab sink, heated bath

750 g KOH : 1500 ml H_2O; many concentrations of KOH may be used to give faster/slower etch rates and higher/lower selectivity of silicon over oxide

Temperature 80°C

Q. OXIDE REMOVAL WET ETCHING

Use lab sink

Etch in diluted HF or buffered HF until desired oxide is removed

Rinse in deionized water for approximately one hour

R. NEAR VERTICAL WALLED TRENCH ETCH

Use inductively coupled plasma etcher

Advanced silicon etch process

High plasma density low pressure processing system

Fluorine plasma

Etch to desired depth

S. **OXIDE, PSG, AND SILICON NITRIDE ETCH**

Use lab sink

Concentrated HF dip with surfactant if needed, continue until desired sacrificial material has been removed

Rinse for 2 minutes in two tanks of DI water

Rinse for 120 minutes in third tank of DI water

T. **SPUTTER GOLD**

Use low pressure chamber

Gold target

U. **GOLD ETCH**

Use lab sink

Aqua regent etchant or other commercially available gold etchant

V. **WET OXIDATION**

Use horizontal atmospheric pressure reactor

Conditions = Temperature as specified, water vapor environment

W. **BORON DIFFUSION**

Use horizontal atmospheric pressure reactor

Solid source boron diffusion

Conditions = Temperature as specified

X. **DEPOSIT *IN SITU* DOPED POLYSILICON**

Use horizontal low pressure chemical vapor deposition reactor

Target thickness as specified

Conditions = 610°C and 300 mTorr

Y. **GROW THERMAL OXIDE**

Use horizontal atmospheric pressure reactor

Conditions = 1050° C, steam environment

Z. **FUSION BOND WAFERS**

Horizontal atmospheric pressure reactor

Conditions = 1100°C, nitrogen environment

EXAMPLE I

Figs. 9a-9e illustrate the process flow for constructing an isotropically etched probe fabricated on a Silicon On Insulator (SOI) wafer. Fig. 9a illustrates an SOI wafer 90 including an insulator layer 92 sandwiched between a device wafer 94 and a handle wafer 96. The device wafer 94 is formed of single crystal silicon with a thickness of approximately 100 μm. The orientation is (100) or (110). The insulator 92 is thermally grown SiO_2, which is 1 to 2 μm thick, but may also be silicon nitride and/or chemically deposited oxide. The handle wafer 96 is approximately 500 μm thick single crystal silicon with a (100) orientation. Since the handle wafer 96 is formed of single crystal silicon it has the same hatching as the device wafer 94, which is also formed of single crystal silicon.

After the wafer 90 is cleaned (step A), an approximately 0.5 μm thick layer of silicon nitride (step D) is deposited. The silicon nitride 98, shown in Fig. 9b, serves as the masking material for the silicon isotropic etch. The silicon nitride 98 is then patterned (step H), etched (step L), and the photoresist is stripped (step K). The resulting structure is shown in Fig. 9c. The device is subsequently submerged in the isotropic silicon etchant (step O), producing the device shown in Fig. 9d. Observe that this operation produces smooth side walls 36 and 38 of the type shown in Figs. 1-5. It should be appreciated that Figs. 9a-9e are a front cross-sectional view of the probe 20 in approximately the center of the elongated body 22. The same processing generates the previously disclosed tip 40.

The silicon nitride is then removed and the probe is released (step S). Fig. 9e illustrates the released probe 20. The device is then rinsed in deionized water for

approximately one hour. The resultant device, which does not include a channel, is a probe for use as a lancet.

EXAMPLE II

Figs. 10a-10i illustrate the process flow to construct an isotropically etched probe with a surface micromachined fluid channel fabricated on an SOI wafer. Fig. 10a illustrates a device of the type shown and described in reference to Fig. 9a. The wafer is cleaned (step A). Then, an approximately 2 μm thick layer of phosphosilicate glass is deposited (step E). Fig. 10b shows the phosphosilicate glass 100, which is used as the sacrificial channel material. The phosphosilicate glass 100 is then patterned (step H), etched (step J), and the photoresist is stripped (step K) to form the mold to make the fluid channel. The resultant device is shown in Fig. 10c. The device is then cleaned (step B) and an approximately 2 μm layer of polysilicon is deposited (step M) to form the frame material of the channel cap. The polysilicon 102 is shown in Fig. 10d. The polysilicon 102 is then patterned (step H), etched (step N), and the resist is stripped (step K). This results in the previously described channel cap inlet port and the channel cap outlet port. In addition, this operation removes the polysilicon away from the edge of the shell. The resultant structure is shown in Fig. 10e. The region 32 between the two polysilicon 102 members is the channel cap outlet port.

The wafer is then cleaned (step B). A 0.5 μm thick layer of silicon nitride is then deposited (step D). The silicon nitride 98, shown in Fig. 10f, operates as the masking material for the silicon isotropic etch. The silicon nitride 98 is then patterned (step H), etched (step L), and the resist is stripped (step K), resulting in the device shown in Fig. 10g.

The device is then submerged in an isotropic silicon etchant (step O), producing the device shown in Fig. 10h. Once again observe the first and second curved side walls 36 and 38 formed by this operation. This operation also produces the previously described tip structure.

The silicon nitride is then removed (step S), the probe is released, and the phosphosilicate glass is removed to produce the device shown in Fig. 10i. The device is then rinsed in deionized water for approximately one hour.

EXAMPLE III

Figs. 11a-11L illustrate process flow for an isotropically shaped probe incorporating an anisotropic etch to form a channel, as fabricated on an SOI wafer. The starting device of Fig. 11a is of the type described in the previous examples. The wafer is cleaned (step A) and approximately 0.5 μm of silicon nitride is deposited (step D), resulting in the device shown in Fig. 11b. Alternately, a 0.5 μm thick layer of thermal oxide can replace the 0.5 μm thick layer of silicon nitride. The oxide layer is etched using CF_4+CHF_3 +He plasma etch and 4:1 H_2O:KOH solution at 40°C. The silicon nitride is then patterned (step H), etched (step L), and the resist is stripped (step K). The single crystal silicon (100) is then subjected to an anisotropic etchant (step P) to form an anisotropically etched trench 72 for a fluid passage, as shown in Fig. 11c.

The wafer is then cleaned (step A) and approximately 2 μm of phosphosilicate glass is deposited (step E) to fill openings in the silicon nitride masking layer 98, as shown in Fig. 11d. It may be preferable to perform a 3 μm thick deposition of PSG and a higher temperature densification of the PSG than is specified by Step G. A more suitable densification is 2 hours, 1100°C in an ambient stream. Since it is desirable to minimize the high temperature steps in cases where circuitry is involved, a densification at temperatures closer to 950°C should be done. The phosphosilicate glass 100 is then patterned (step H), etched (step J), and the resist is stripped (step K) to expose regions of the silicon nitride 98, as shown in Fig. 11e.

The silicon nitride 98 is then etched (step L), resulting in the device shown in Fig. 11f. The resist can typically be removed before the nitride etch since the phosphosilicate glass acts as an etch mask. In some cases, the thickness of the phosphosilicate glass may not be thick enough to prevent the etch from attacking the underlying nitride, in which case, photoresist may be necessary.

The wafer is then cleaned (step B). Approximately 2 μm of polysilicon is then deposited (step M) to form the frame material of the channel cap, resulting in the device shown in Fig. 11g. The device is then patterned (step H), etched (step N), and the photoresist is stripped (step K) to form the channel cap inlet and outlet ports and to remove the polysilicon away from the edge of the shell. This processing results in the device shown in Fig. 11h. The wafer is then cleaned (step B) and approximately 0.5 μm of silicon nitride is deposited (step D). The silicon nitride 98, as shown in Fig. 11i, is used as the masking material for the silicon isotropic etch.

The silicon nitride is then patterned (step H), etched (step L), and the resist is stripped (step K), resulting in the structure shown in Fig. 11j. The device is then submerged in an isotropic silicon etchant (step O), producing the structure of Fig. 11k. The silicon nitride is then removed, the probe is released, and the phosphosilicate glass is removed (step S). The resulting device, shown in Fig. 11L is then rinsed in deionized water for approximately one hour.

EXAMPLE IV

Figs. 12a-12L illustrate process flow for an isotropically shaped probe incorporating an isotropic etch to form a channel, as fabricated on an SOI wafer. The starting device of Fig. 12a is of the type described in the previous examples. The wafer is cleaned (step A) and approximately 0.5 μm of silicon nitride is deposited (step D), resulting in the device shown in Fig. 12b. The silicon nitride is then patterned (step H), etched (step L), and the resist is stripped (step K). The single crystal silicon (100) is then subjected to an isotropic etchant (step O) to form an isotropically etched flat-bottom trench 74 for a fluid passage, as shown in Fig. 12c.

The wafer is then cleaned (step A) and approximately 2 μm of phosphosilicate glass is deposited (step E) to fill openings in the silicon nitride masking layer 98, as shown in Fig. 12d. The phosphosilicate glass 100 is then patterned (step H), etched (step J), and the resist is stripped (step K) to expose regions of the silicon nitride 98, as shown in Fig. 12e.

The silicon nitride 98 is then etched (step L), resulting in the device shown in Fig. 12f. The resist can typically be removed before the nitride etch since the phosphosilicate glass acts as an etch mask. In some cases, the thickness of the phosphosilicate glass may not be thick enough to prevent the etch from attacking the underlying nitride, in which case, photoresist may be necessary.

The wafer is then cleaned (step B). Approximately 2 μm of polysilicon are then deposited (step M) to form the frame material of the fluid channel, resulting in the device shown in Fig. 12g. The device is then patterned (step H), etched (step N), and the photoresist is stripped (step K) to form the fluid inlet and outlet port and to remove the polysilicon away from the edge of the shell. This processing results in the device shown in Fig. 12h. The wafer is then cleaned (step B) and approximately 0.5 μm of

silicon nitride is deposited (step D). The silicon nitride 98, as shown in Fig. 12i, is used as the masking material for the silicon isotropic etch.

The silicon nitride is then patterned (step H), etched (step L), and the resist is stripped (step K), resulting in the structure shown in Fig. 12j. The device is then submerged in an isotropic silicon etchant (step O), producing the structure of Fig. 12k. The silicon nitride is then removed, the probe is released, and the phosphosilicate glass is removed (step S). The resulting device, shown in Fig. 12L is then rinsed in deionized water for approximately one hour.

EXAMPLE V

Figs. 13a-13q' illustrate the process flow for an isotropically shaped probe incorporating an anisotropic etch to form a channel fabricated on an SOI wafer with integrated circuitry and a micromachined structure in the form of a polysilicon heater. In the following figures, the figures on the left-hand side of each page are cross-sections of the shaft, while the figures on the right-hand side of each page are cross-sections of the circuitry. Fig. 13a is a SOI wafer with (100) orientation. The left side of Fig. 13a' illustrates two p+ doped regions 120 and 122. A polysilicon contact 124 is positioned above each region. An n+ polysilicon region 126 is positioned between the contacts 124. The right side of Fig. 13a' has a similar configuration, but further includes an n well 130 and n+ regions 132. The processing used to construct a device of this type is known in the art.

The wafer is cleaned (step B) and approximately 0.5μm of silicon nitride is deposited (step D.), resulting in the structure shown in Figs. 13b and 13b'. The wafer is then cleaned (step B) and approximately 0.4 μm of polysilicon is deposited (step X) to form a polysilicon heater. The polysilicon is patterned (step H), etched (step N), and the resist is stripped (step K). The wafer is then cleaned (step B). Approximately 0.5 μm of silicon nitride is then deposited (step D) to protect the polysilicon during the silicon etch. The resultant structure is shown in Figs. 13c and 13c'.

The silicon nitride is then patterned (step H), etched (step L), and the resist is stripped (step K). (A more IC compatible etch of tetramethyl ammonium hydroxide may be used in lieu of KOH). The single crystal silicon is then etched in an anisotropic etch (step P) to form a trench for a fluid passage, as shown in Fig. 13d. The wafer is then cleaned (step A) and approximately 2 μm of phosphosilicate glass is

deposited (step E) to fill openings in the silicon nitride mask layer. The resultant structure is shown in Figs. 13e and 13e'.

The device is then patterned (step H), etched (step J), and the resist is stripped (step K). This exposes regions of the silicon nitride, as shown in Figs. 13f and 13f'. The silicon nitride is then patterned (step H), etched (step L), and the resist is stripped (step K). This operation removes the nitride from the region outside of the channel and over the electrical contact holes, as shown in Figs. 13g and 13g'.

The wafer is then cleaned (step B) and approximately 2 μm of polysilicon (step M) is deposited to form the frame material of the fluid channel, as shown in Figs. 13h and 13h'. The polysilicon is then patterned (step H), etched (step N), and resist is stripped (step K). This operation produces channel cap inlet and outlet ports and removes the polysilicon away from the edge of the shell. The resultant structure is shown in Figs. 13i and 13i'.

The wafer is then cleaned (step B) and approximately 0.4 μm of polysilicon is deposited (step M) to form a thin, protective layer over the electrical contacts during a subsequent HF etch. This results in the structure of Figs. 13j and 13j'. The polysilicon is then patterned (step H), etched (step N), and the resist is stripped (step K). This results in the removal of the polysilicon that is not covering the circuitry, as shown in Figs. 13k and 13k'.

The wafer is then cleaned (step B) and approximately 0.5μm of silicon nitride is deposited (step D). The silicon nitride, shown in Figs. 13L and 13L', is used as the masking material for the silicon isotropic etch. The silicon nitride is then patterned (step H), etched (step L), and the resist is stripped (step K). This results in the structure of Figs. 13m and 13m'. The device is then submerged in isotropic silicon etchant (step O), producing the structure of Figs. 13n and 13n'.

The wafer is then submerged in HF (step S), to remove most of the silicon nitride, release the probe, and to remove phosphosilicate glass. The resulting structure is shown in Figs. 13o and 13o'. Some silicon nitride should remain to insulate the heaters from the substrate so timing of the HF etch is important. The wafer is then rinsed in deionized water for approximately one hour.

A short silicon plasma etch (step N) is then performed to remove the thin, protective layer of polysilicon over the circuitry. This operation results in the device of Figs. 13p and 13p'. The final step is a quick dip in hydroflouric acid to remove the

oxide covering the polysilicon contacts (step Q). The final structure is shown in Figs. 13q and 13q'.

EXAMPLE VI

Figs. 14a-14m' illustrate the process flow for an isotropically shaped probe incorporating an anisotropic etch to form a channel. The process utilizes a thin wafer with circuitry and double sided etching. In the following figures, the figures on the left-hand side of each page are cross-sections of the probe shaft, while the figures on the right-hand side of each page are cross-sections of the circuitry. Fig. 14a shows a (100) silicon p-type wafer that is approximately 100 μm thick. Fig. 14a' shows a structure of the type described in reference to Fig. 13a', but without layers 92 and 96 of Fig 13a'.

The wafer is cleaned (step B). Approximately 0.5 μm of silicon nitride is then deposited (step D). The resultant structure is shown in Figs. 14b and 14b'. The silicon nitride is then patterned (step H), etched (step L), and the resist is stripped (step K). The single crystal silicon is then etched in an anisotropic etchant (step P) to form the trench for the fluid passage. The resultant structure is shown in Figs. 14c and 14c'.

The wafer is then cleaned (step A) and approximately 2 μm of phosphosilicate glass is deposited (step E) to fill openings in the silicon nitride masking layer. The resultant structure is shown in Figs. 14d and 14d'. The phosphosilicate glass is then patterned (step H), etched (step J), and the resist is stripped (step K). This results in the formation of a mold to make the fluid channel cap. The silicon nitride is then etched (step L). The resultant structure is shown in Figs. 14e and 14e'. The resist can typically be removed before the nitride etch since the phosphosilicate glass acts as an etch mask. In some cases, the thickness of the phosphosilicate glass may not be thick enough to prevent the etch from attacking the underlying nitride, in which case photoresist may be necessary.

The wafer is then cleaned (step B) and approximately 2 μm of polysilicon is deposited (step M) to form the frame material of the fluid channel. The resultant structure is shown in Figs. 14f and 14f'. The polysilicon is then patterned (step H) and etched (step N) to form the fluid inlet and outlet ports and to remove the polysilicon away from the edge of the shell. The polysilicon is then removed from the back side

of the wafer (step N) and the resist is stripped (step K). The resultant structure is shown in Figs. 14g and 14g'.

The wafer is then cleaned (step B) and approximately 0.5 μm of silicon nitride is deposited (step D) to function as a masking material for the silicon isotropic etch. Figs. 14h and 14h' show the resultant structure. The silicon nitride is then patterned (step H), etched (step L), and the resist is stripped (step K), to generate the structure shown in Figs. 14i and 14i'. The silicon nitride of the electrical contacts is then patterned (step H) and the silicon nitride layer is etched (step L), the polysilicon layer is etched (step N), the silicon nitride layer is etched (step L), and the oxide layer is etched (step Q), to expose the electrical contacts as shown in Fig. 14j'. The resist is then stripped (step K).

The wafer is then cleaned (step B) and gold is sputtered (step T) on the front side of the wafer. Preferably, a chromium adhesion layer is used. The gold is patterned (step H), etched (step U), and the resist is stripped (step K). The resultant gold pockets are shown in Fig. 14k'. The wafer is then submerged in an isotropic etchant (step O), producing the structure of Figs. 14l and 14l'. The wafer is then submerged in HF (step S) to remove the silicon nitride, release the probe, and remove the phosphosilicate glass. The wafer is then rinsed in deionized water for approximately one hour to produce the structure shown in Figs. 14m and 14m'.

EXAMPLE VII

Figs. 15a-15m' illustrate the process flow for an isotropically shaped probe incorporating an anisotropic etch to form a channel. The process utilizes a standard thickness wafer with circuitry and double sided etching. In the following figures, the figures on the left-hand side of each page are cross-sections of the probe shaft, while the figures on the right-hand side of each page are cross-sections of the circuitry. Fig. 15a shows a (100) silicon p-type wafer that is approximately 500 μm thick. Fig. 15a' shows a structure of the type described in reference to Fig. 13a', but without layers 92 and 96 of Fig 13a'.

The wafer is cleaned (step B) and approximately 0.5 μm of silicon nitride is deposited (step D), resulting in the structure of Figs. 15b and 15b'. The silicon nitride is then patterned (step H), etched (step L), and the resist is stripped (step K). The

single crystal silicon is then etched in an anisotropic etchant (step P) to form a fluid passage trench, as shown in Fig. 15c.

The wafer is then cleaned (step B) and approximately 2 μm of phosphosilicate glass is deposited (step E) to fill openings in the silicon nitride masking layer. The resultant structure is shown in Figs. 15d and 15d'. The phosphosilicate glass is then patterned (step H), etched (step J), and the resist is stripped (step K). This forms the mold to make the fluid channel cap. The silicon nitride is then etched (step L), resulting in the structure shown in Figs. 15e and 15e'. The resist can typically be removed before the nitride etch since the phosphosilicate glass acts as an etch mask. In some cases, the thickness of the phosphosilicate glass may not be thick enough to prevent the etch from attacking the underlying nitride in which case, photoresist may be necessary.

The wafer is then cleaned (step B) and approximately 2 μm of polysilicon is deposited (step M) to form the frame material, as shown in Figs. 15f and 15f'. The polysilicon is then patterned (step H) and etched (step N) to form the channel cap inlet and outlet port, to remove the polysilicon away from the edge of the shell, and to remove polysilicon from the back side of the wafer (step N). The resist is then stripped (step K). The resultant structure is shown in Figs. 15g and 15g'.

The wafer is then cleaned (step B) and approximately 0.5 μm of silicon nitride is deposited (step D). The silicon nitride serves as the masking material for the silicon isotropic etch. The silicon nitride layer is shown in Figs. 15h and 15h'. The silicon nitride is patterned (step H), etched (step L), and the resist is stripped (step K). This results in the structure shown in Figs. 15i and 15i'.

A pattern is then applied over the electrical contacts (step H). The silicon nitride layer is then etched (step L), the polysilicon layer is etched (step N), the silicon nitride layer is etched (step L), and the oxide layer is etched (step Q). The resist is then stripped (step K). The resultant structure is shown in Figs. 15j and 15j'.

The wafer is then cleaned (step B) and gold is sputtered (step T) onto the front side of the wafer. The gold is patterned (step H), etched (step U), and the resist is stripped (step K), to yield the structure of Figs. 15k and 15k'. Additional adhesion layers such as titanium or chromium may be necessary to be deposited before the gold deposition.

The wafer is then submerged in an isotropic silicon etchant (step O), to produce the structure of Figs. 15l and 15l'. The wafer is then submerged in HF (step S) to remove silicon nitride, release the probe, and remove phosphosilicate glass. The wafer is then rinsed in deionized water for approximately one hour. The final structure is shown in Figs. 15m and 15m'.

EXAMPLE VIII

Figs. 16a-16o' illustrate the process flow for an anisotropically and isotropically shaped probe incorporating an anisotropic etch to form the channel. The device is fabricated on an SOI wafer with a (110) top layer. The processing is used to construct a device of the type shown in Figs. 6-7. The figures on the left-hand side of the page show the cross-section of the tip region, while the figures on the right-hand side of the page show the cross-section of the probe shaft region.

Figs. 16a and 16a' show a (110) silicon wafer bonded to oxide on a silicon wafer. The wafer is cleaned (step A) and approximately 0.5 μm of silicon nitride is deposited (step D), resulting in the device shown in Figs. 16b and 16b'. The silicon nitride is then patterned (step H), etched (step L), and the resist is stripped (step K). The single crystal silicon is then subject to an anisotropic etchant (step P) to form the trench for the fluid passage, resulting in the device of Figs. 16c and 16c'.

The wafer is then cleaned (step A) and approximately 2 μm of phosphosilicate glass is deposited (step E) to fill openings in the silicon nitride masking layer, as shown in Figs 16d and 16d'. The phosphosilicate glass is then patterned (step H), etched (step J), and the resist is stripped (step K). This operation exposes regions of the silicon nitride, as shown in Figs. 16e and 16e'. The silicon nitride is then etched (step L) to produce the structure of Figs 16f and 16f'. The resist can typically be removed before the nitride etch since the phosphosilicate glass acts as an etch mask. In some cases, the thickness of the phosphosilicate glass may not be thick enough to prevent the etch from attacking the underlying nitride, in which case photoresist may be necessary.

The wafer is then cleaned (step B) and approximately 2 μm of polysilicon is deposited (step M) to form the frame material of the fluid channel. The resultant structure is shown in Figs. 16g and 16g'. The polysilicon is then patterned (step H)

and etched (step N) to form the channel cap inlet and outlet ports. The resist is then stripped (step K). This results in the device of Figs. 16h and 16h'.

The wafer is then cleaned (step B) and approximately 0.5 μm of silicon nitride (step D) is deposited, as shown in Figs. 16i and 16i'. The silicon nitride operates as the masking material for the silicon isotropic etch. The silicon nitride is patterned (step H), etched (step L), and the resist is stripped (step K). This results in the structure of Figs. 16j and 16j'.

The wafer is then cleaned (step A) and approximately 2 μm of low temperature oxide (step F) is deposited for the anisotropic etch masking material. An alternative masking material is polyhexane or even an additional layer of silicon nitride. The deposited substance is patterned (step H), etched (step J), and the resist is stripped (step K) to yield the structure of Figs. 16k and 16k'.

The single crystal silicon is then etched in an anisotropic etchant (step P) to form vertical walls along the shaft of the probe, as shown in Figs. 16l and 16l'. The low temperature oxide anisotropic silicon etchant mask is then removed (step Q), to generate the structure of Figs. 16m and 16m'.

The wafer is then submerged in an isotropic silicon etchant (step O) to produce smooth, converging surfaces at the tip, as shown in Fig. 16n. The wafer is then submerged in HF (step S) to remove silicon nitride, release the probe, and remove the phosphosilicate glass, as shown in Figs. 16o and 16o'. The wafer is then rinsed in deionized water for approximately one hour.

The techniques of the invention may also be used in connection with non-SOI, standard thickness wafers. The expense of SOI wafers and thin wafers is approximately four times that of standard wafers. Therefore, it is desirable to use standard wafers, yet retain the geometry control provided by SOI and thin wafers. Standard thickness wafer processing discussed below does not apply to double sided etched devices of the type described above.

The processing of standard thickness, non-SOI wafers involves a grind step and a chemical mechanical polish. Figure 17 illustrates a basic process flow. Figure 18 illustrates an alternate process flow with an additional step. The additional step is an oxidation that assists in the chemical mechanical polishing process by providing an etch stop. Having an etch stop improves the uniformity of the shapes of the probes. A third process flow is shown in Figure 19. This process flow has an additional step of a

temporary bond to a plain, standard wafer. The purpose of the bond is to rigidly fix the probes during the grinding and polishing steps. There is a possibility that during the grinding and polishing steps that the probes may not be held sufficiently tight using only adhesives and that a stronger bond, like that supplied by an oxide to oxide fusion bond, may be necessary. Otherwise, if the probes were to move during the grinding and polishing steps, their sharpness may be decreased. The standard wafer used for the temporary fusion bond should be able to be reused many times. Therefore, it does not add significant cost.

Example IX

A single crystal (100) silicon p-type wafer approximately 500 μm thick is used as a starting wafer 110, as shown in Figure 17(a). The wafer is cleaned (step A) and approximately 0.5μm of silicon nitride (step D) is deposited. The deposited silicon nitride 112 is shown in Figure 17(b). The silicon nitride is used as the masking material for the silicon isotropic etch.

The silicon nitride is then patterned (step H), etched (step L), and the resist is stripped (step K), producing the device of Figure 17(c). The wafer is then submerged in an isotropic silicon etchant (step O), producing the device of Figure 17(d). The wafer is then submerged in HF (step S) to remove the silicon nitride, resulting in the device of Figure 17(e). The wafer is then rinsed in deionized water for approximately 15 minutes. The majority of the silicon wafer is then grinded off to within a few micrometers of the bottom of the etched region. Then, using chemical mechanical polishing, the bottom of the wafer is polished until sharp structures are formed. The final device is shown in Figure 17(f).

Example X

A single crystal (100) silicon p-type wafer approximately 500 μm thick is used as a starting wafer 110, as shown in Figure 18(a). The wafer is cleaned (step A) and approximately 0.5μm of silicon nitride (step D) is deposited. The deposited silicon nitride 112 is shown in Figure 18(b). The silicon nitride is used as the masking material for the silicon isotropic etch.

The silicon nitride is then patterned (step H), etched (step L), and the resist is stripped (step K), producing the device of Figure 18(c). The wafer is then submerged

in an isotropic silicon etchant (step O), producing the device of Figure 18(d). The wafer is then submerged in HF (step S) to remove the silicon nitride, resulting in the device of Figure 18(e).

The wafer is then cleaned (step A) and a 1 μm thick layer of SiO_2 is thermally grown (step Y). The oxide layer 114 is shown in Figure 18(f). The majority of the silicon wafer is then grinded off to within a few micrometers of the bottom of the etched region. Then, using chemical mechanical polishing, the bottom of the wafer is polished until sharp structures are formed. The resultant device is shown in Figure 18(g). The wafer is then submerged in HF (step S) to remove the oxide. The wafer is finally rinsed in deionized water for approximately 15 minutes, resulting in the device of Figure 18(h).

Example XI

A single crystal (100) silicon p-type wafer approximately 500 μm thick is used as a starting wafer 110, as shown in Figure 19(a). The wafer is cleaned (step B) and approximately 0.5μm of silicon nitride (step D) is deposited. The deposited silicon nitride 112 is shown in Figure 19(b). The silicon nitride is used as the masking material for the silicon isotropic etch.

The silicon nitride is then patterned (step H), etched (step L), and the resist is stripped (step K), producing the device of Figure 19(c). The wafer is then submerged in an isotropic silicon etchant (step O), producing the device of Figure 19(d). The wafer is then submerged in HF (step S) to remove the silicon nitride, resulting in the device of Figure 19(e). The wafer is then cleaned (step A) and a 1 μm thick layer of SiO_2 is thermally grown (step Y). The oxide layer 114 is shown in Figure 19(f).

At this point, the thermally oxidized wafer 110 is bonded (step Z) to a standard, plain thermally oxidized wafer that has an approximately 1 μm thick layer of SiO_2 thermally grown thereon (step Y). Figure 19(g) illustrates the wafer 110 bonded to a handle wafer 120, which has oxide layer 122. The wafer 110 is then grinded to within a few micrometers of the bottom of the etched region. The wafer is then chemical mechanically polished until sharp structures are formed. The resultant device is shown in Figure 19(h). The wafer is then submerged in HF (step S) to remove the oxide and the handle wafer. The wafer is then rinsed in deionized water for approximately 15 minutes, resulting in the device of Figure 19(i).

Example XII

In one embodiment of the invention, the shape of the tip is controlled through adjustments in the deposition conditions of a layer of phosphosilicate glass, which is sandwiched between a silicon nitride masking layer and the SOI device layer. By incorporating a layer of phosphosilicate glass between the masking layer and the single crystal silicon, the tip geometry can be controlled by changing the phosphorous doping of the phosphosilicate glass. The phosphosilicate glass can be used to prevent unwanted tip hooking.

Figure 20(a) illustrates an SOI wafer 90 including an insulator layer 92 sandwiched between a device wafer 94 and a handle wafer 96. The device 94 is formed of single crystal silicon with a thickness of approximately 100 μm. The orientation is (100) or (110). The insulator 92 is thermally grown SiO_2, which is 1 to 2 μm thick, but may also be silicon nitride and/or chemically deposited oxide. The handle wafer 96 is 500 μm thick single crystal silicon with a (100) orientation.

Approximately 800 nanometers of phosphosilicate glass is deposited (step E) on the wafer. Figure 20(b) illustrates the phosphosilicate glass layer 130. Low-stress silicon nitride is then deposited on the wafer (step D). Figure 20(c) illustrates the deposited layer 132.

The silicon nitride layer 132 is then patterned (step H). Afterwards, the silicon nitride layer is etched (step L) and the phosphosilicate glass layer is etched (step J). This results in the device of Figure 20(d). The silicon is then wet etched (step O), producing the device of Figure 20(e). Finally, an HF release is performed (step S), producing the released device shown in Figure 20(f).

The PSG reduces the incidence of tip hooks being formed. The tip hook problem occurs when the probe shape etch mask of low-stress silicon nitride is deposited directly onto silicon. The PSG placed between the silicon nitride and the silicon etches faster than the silicon. This faster etching material erodes during the etching process and therefore solves the silicon hooking problem.

The etch rate of PSG was measured for a variety of phosphine flow rates. The etch rate results for wafers with PSG having PH_3 flow rates of 0.0, 1.2, 2.4, 3.6, and 4.8 sccm are shown in Figure 21. Also shown in Figure 21 is a horizontal line at 1100 Å/min which was the etch rate found for single crystal silicon. Based on the measured

etch rates, PSG is a highly desirable material to correct the hooking problem, since its etch rate ratio to silicon can be tailored to be from 0.1 to over 4.3.

Figures 22A and 22B illustrate probes 140 and 141 constructed in accordance with any number of the example processes described herein. The probes do not include a channel and therefore are considered to be lancets or blades. The probes may be connected to larger structures to facilitate their use as lancets or blades. The probe 140 of Figure 22A has an isotropically etched tip formed on one side of the device, while the probe 141 of Figure 22B has an isotropically etched tip formed on both sides of the device.

Figure 23 illustrates a matrix of isotropically etched tips constructed in accordance with an embodiment of the invention. The matrix 150 is formed on a semiconductor substrate 152. More particularly, the matrix 150 is formed on a planar surface of the substrate 152. The device 150 may be used as an "abrader". That is, the device may be used to abrade the epidermis to facilitate transdermal drug delivery. Figure 24 is an enlarged view of individual isotropically etched tips 154 of the matrix 150. The tips have typical heights from 20 μm to 350 μm. The minimum spacing between the points is determined by their height. Typical spacings are between two times the height to over ten times the height. All of the points are fabricated using standard wafers. Three process are discussed below. The first process results in devices with sharp points. In some cases, these sharp points can break during use due to the small cross-section at the tips. Hence, two other processes are included to form arrays having duller points which are more durable. The first alternative process is accomplished by simply stopping the isotropic etch prematurely. The resulting structures have a flat-top rather than a point. The second alternative process is accomplished by the addition of a PSG layer between the silicon nitride masking layer. The resulting structures have a pyramid-like shape.

Example XIII

A single crystal (100) silicon wafer approximately 500 μm thick is used as a starting wafer 110, as shown in Figure 25(a). The wafer is cleaned (step B) and approximately 0.5μm of silicon nitride (step D) is deposited. The deposited silicon nitride 112 is shown in Figure 25(b). The silicon nitride is used as the masking material for the silicon isotropic etch.

The silicon nitride is then patterned (step H), etched (step L), and the resist is stripped (step K), producing the device of Figure 25(c). The wafer is then submerged in an isotropic silicon etchant (step O) until sharp points are formed, as shown in Figure 25(d). The wafer is then rinsed in deionized water for approximately 15 minutes. Afterwards, the wafer is submerged in HF (step S) to remove the silicon nitride. Finally, the wafer is rinsed in deionized water for approximately 15 minutes, producing the device shown in Figure 25(e).

Example XIV

A single crystal (100) silicon wafer approximately 500 μm thick is used as a starting wafer 110, as shown in Figure 26(a). The wafer is cleaned (step B) and approximately 0.5μm of silicon nitride (step D) is deposited. The deposited silicon nitride 112 is shown in Figure 26(b). The silicon nitride is used as the masking material for the silicon isotropic etch.

The silicon nitride is then patterned (step H), etched (step L), and the resist is stripped (step K), producing the device of Figure 26(c). The wafer is then submerged in an isotropic silicon etchant (step O) and is subsequently removed before sharp points are formed. This processing results in the device of Figure 26(d). The wafer is then rinsed in deionized water for approximately 15 minutes. Afterwards, the wafer is submerged in HF (step S) to remove the silicon nitride. Finally, the wafer is rinsed in deionized water for approximately 15 minutes, producing the device shown in Figure 26(e).

Example XV

A single crystal (100) silicon wafer approximately 500 μm thick is used as a starting wafer 110, as shown in Figure 27(a). The wafer is cleaned (step A) and approximately 0.8μm of phosphosilicate glass (PSG) is deposited (step E). The PSG is then densified (step G). Then, 0.5 μm of silicon nitride (step D) is deposited. The deposited silicon nitride 112 and PSG 130 is shown in Figure 27(b). The silicon nitride is used as the masking material for the silicon isotropic etch.

The silicon nitride is then patterned (step H). Afterwards, the silicon nitride and oxide layer is etched (step L), and the resist is stripped (step K), producing the device of Figure 27(c). The wafer is then submerged in an isotropic silicon etchant (step O).

This processing results in the device of Figure 27(d). Afterwards, the wafer is submerged in HF (step S) to remove the silicon nitride and PSG. Finally, the wafer is rinsed in deionized water for approximately 15 minutes, producing the device shown in Figure 27(e).

All of the foregoing examples share the common trait that they result in a device with an isotropically etched tip. The advantage of the disclosed probes over standard stainless steel probes is that they can be made with smaller cross-sections, sharper tips, and can include integrated circuitry or micromachined structures. Small cross-sections and sharper tips result in minimized pain and tissue damage and the integrated circuitry provides a convenient means to incorporate sensing, stimulating, pumping, and valving operations. Unlike prior art probes, the probes of the present invention are constructed without expensive Boron doping. Further, the processing does not require the use of the dangerous carcinogen ethylenediamine pyrocatechol.

Many process variations have been described to result in a variety of shaft cross-sections. In addition, several styles of substrates have been disclosed, including silicon on insulator, thinner than standard silicon wafers, and standard thickness silicon wafers. However, all of the probe variations maintain the desired, high tip sharpness, which results from the isotropic etch.

Although single crystal silicon is the preferred fabrication material, other materials may be utilized, including, but not limited to, stainless steel, aluminum, and titanium. Typically, these materials are not used in their single crystal form so they cannot be used in process flows relying upon highly anisotropic properties.

The silicon probes of the invention may be coated with nickel, titanium, gold, or similar metals which are either sputtered or plated to improve the strength or surface characteristics of the probes. An organic coating, such as Parylene, may also be used for strength enhancement. The probes of the invention may also be thermally oxidized to improve their strength or surface characteristics. Other process variations include the use of an inductively coupled plasma etch to make the vertical side walls of the probe, as shown in Figs. 6 and 7.

The foregoing description, for purposes of explanation, used specific nomenclature to provide a thorough understanding of the invention. However, it will be apparent to one skilled in the art that the specific details are not required in order to practice the invention. In other instances, well known circuits and devices are shown

in block diagram form in order to avoid unnecessary distraction from the underlying invention. Thus, the foregoing descriptions of specific embodiments of the present invention are presented for purposes of illustration and description. They are not intended to be exhaustive or to limit the invention to the precise forms disclosed, obviously many modifications and variations are possible in view of the above teachings. The embodiments were chosen and described in order to best explain the principles of the invention and its practical applications, to thereby enable others skilled in the art to best utilize the invention and various embodiments with various modifications as are suited to the particular use contemplated. It is intended that the scope of the invention be defined by the following Claims and their equivalents.

IN THE CLAIMS:

1. A probe, comprising:
an elongated body with
a top surface,
a bottom surface,
a first side wall between said top surface and said bottom surface,
a second side wall between said top surface and said bottom surface, and
an end defined by said bottom surface converging into a tip, an isotropically etched portion of said first side wall converging into said tip, and an isotropically etched portion of said second side wall converging into said tip.

2. The apparatus of claim 1 wherein said elongated body is less than approximately 700μm wide.

3. The apparatus of claim 1 wherein said elongated body is less than approximately 200μm thick.

4. The apparatus of claim 1 wherein said elongated body is formed of silicon.

5. The apparatus of claim 4 wherein said elongated body is formed of single crystal silicon.

6. The apparatus of claim 5 wherein said elongated body includes a polycrystalline silicon channel cap.

7. The apparatus of claim 4 wherein said elongated body is formed of silicon that is not doped with Boron.

8. The apparatus of claim 1 wherein said elongated body includes integrated circuitry.

9. The apparatus of claim 1 wherein said elongated body includes a micromachined structure.

10. The apparatus of claim 6 wherein said elongated body has a fluid channel formed therein.

11. A method of fabricating a probe, said method comprising the steps of:

providing an elongated body with a top surface, a bottom surface, and a set of sidewalls between said top surface and said bottom surface; and

isotropically etching an end of said elongated body such that said bottom surface converges into a tip and said set of sidewalls converge into said tip.

12. The method of claim 11 wherein said providing step includes the step of providing an elongated body formed of silicon that is not boron doped.

13. The method of claim 11 wherein said providing step includes the step of providing an elongated body formed of a silicon on insulator wafer.

14. The method of claim 11 wherein said providing step includes the step of providing an elongated body that is less than approximately 200μm thick and less than approximately 700μm wide.

15. The method of claim 11 wherein said providing step includes the step of providing a layer of phosphosilicate glass on said top surface to control the etch rate during said etching step and thereby prevent the formation of hook structures adjacent to said tip.

16. The method of claim 11 wherein said etching step includes the step of etching without ethylenediamine pyrocatechol.

17. The method of claim 11 wherein said etching step includes the step of processing said end exclusively at temperatures below approximately 1100°C.

18. The method of claim 11 wherein said etching step includes the step of etching with an anisotropic etchant.

19. The method of claim 11 further comprising the step of forming a fluid channel within said elongated body.

20. The method of claim11 further comprising the step of constructing integrated circuitry on said elongated body.

21. The method of claim 11 further comprising the step of constructing a micromachined structure on said elongated body.

22. A method of fabricating an epidermal abrasion device, said method comprising the steps of:

providing a semiconductor substrate with a planar surface; and

isotropically etching said planar surface to form a matrix of isotropically etched structures on said semiconductor substrate.

23. The method of claim 22 wherein said etching step includes the step of forming a matrix of isotropically etched pointed tips on said semiconductor substrate.

24. The method of claim 22 wherein said etching step includes the step of forming a matrix of isotropically etched flat tips on said semiconductor substrate.

25. The method of claim 22 wherein said etching step includes the step of forming a matrix of isotropically etched pyramids on said semiconductor substrate.

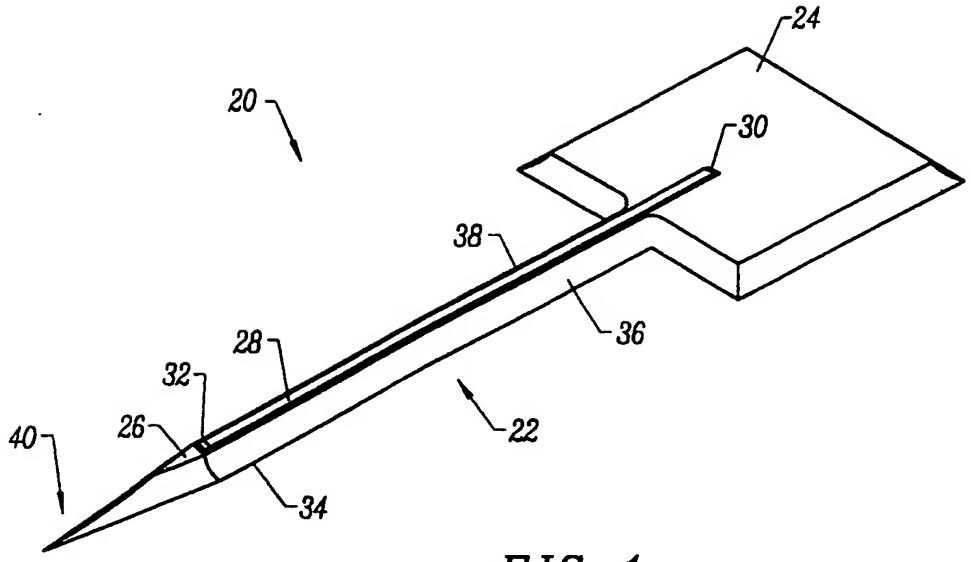

FIG. 1

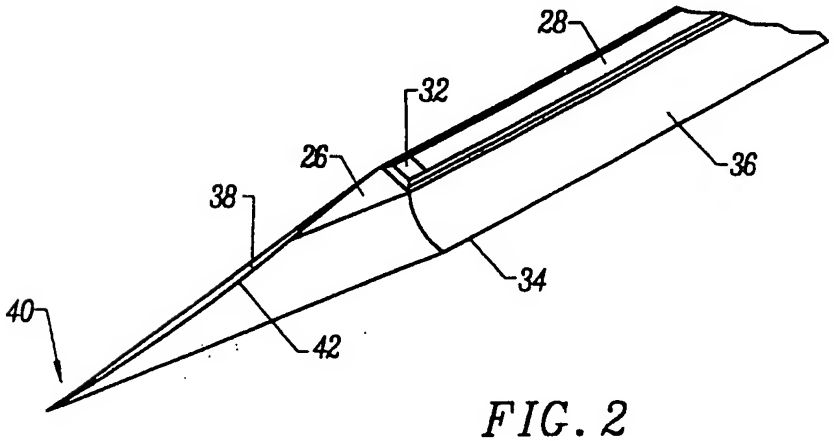

FIG. 2

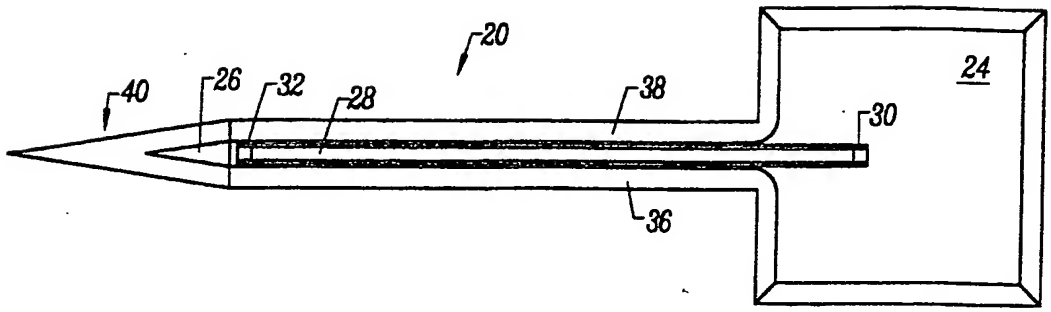

FIG. 3

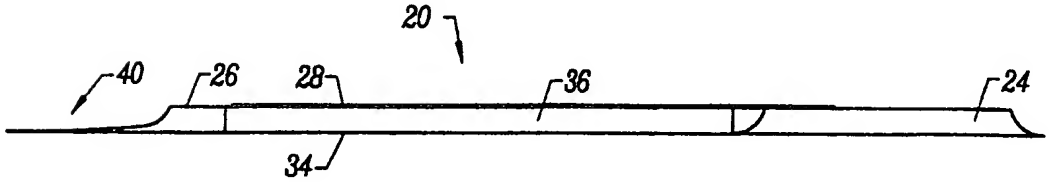

FIG. 4

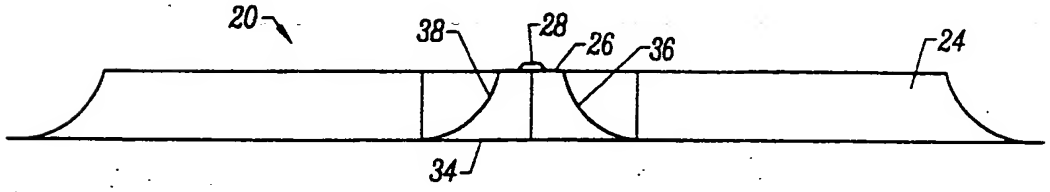

FIG. 5

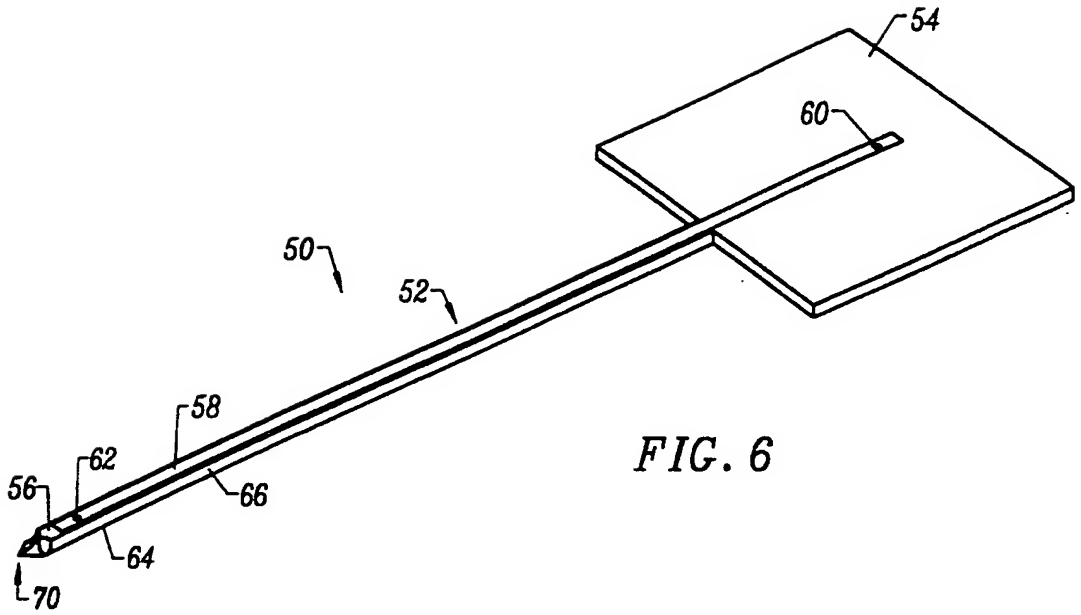

FIG. 6

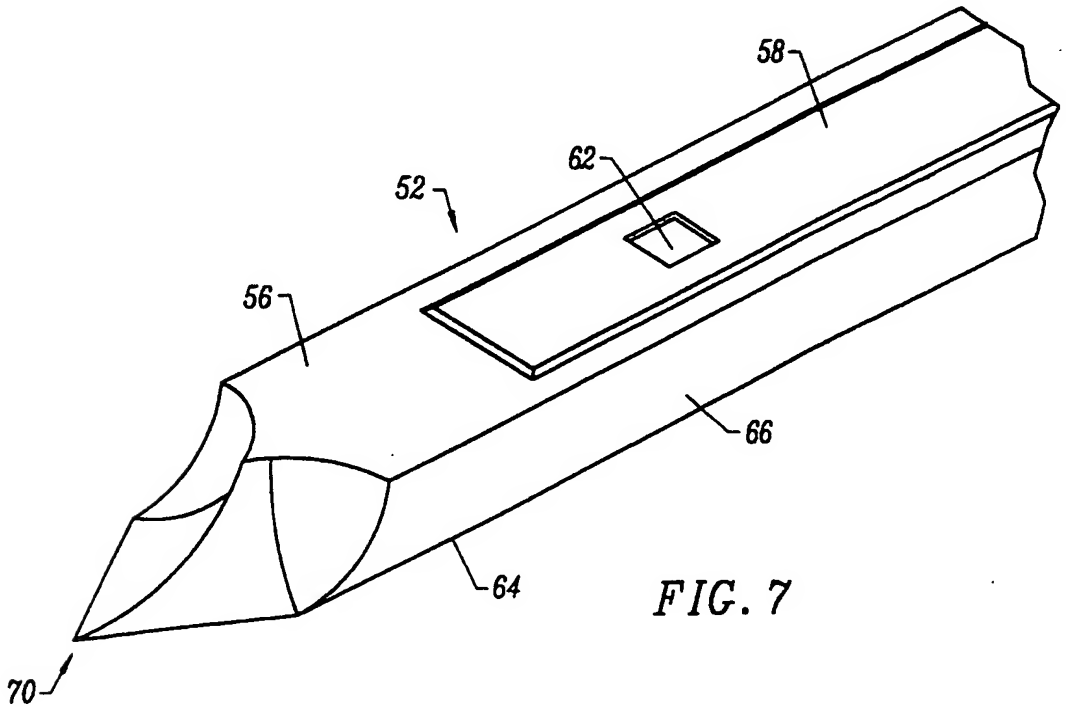

FIG. 7

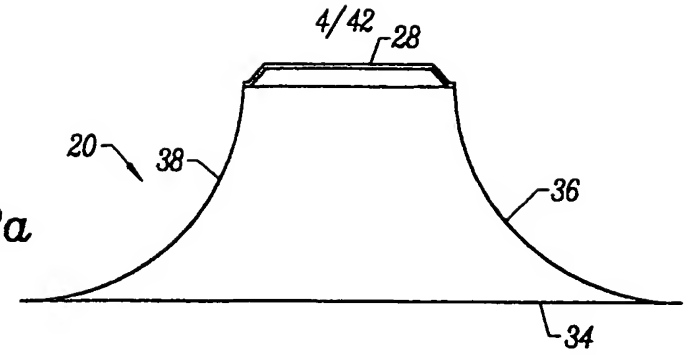

FIG. 8a

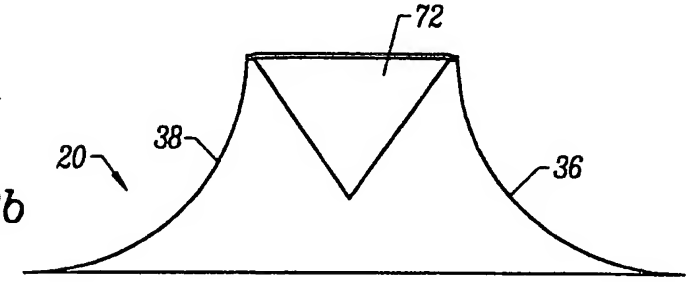

FIG. 8b

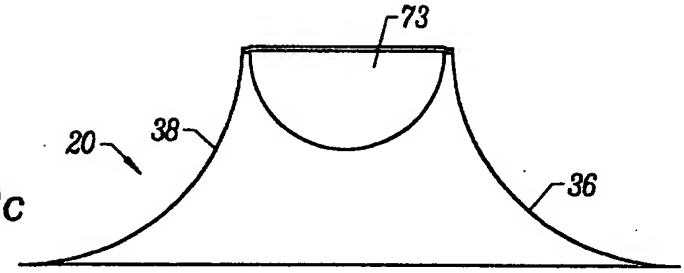

FIG. 8c

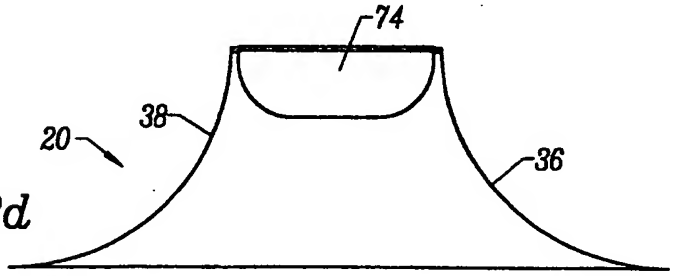

FIG. 8d

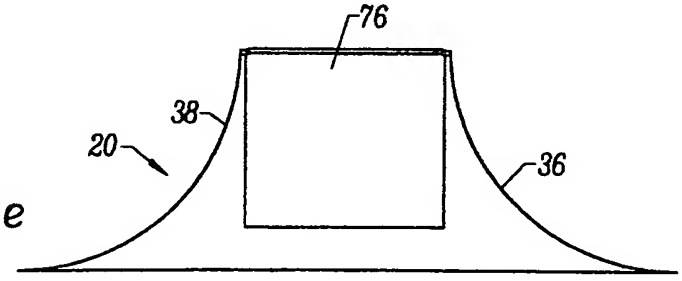

FIG. 8e

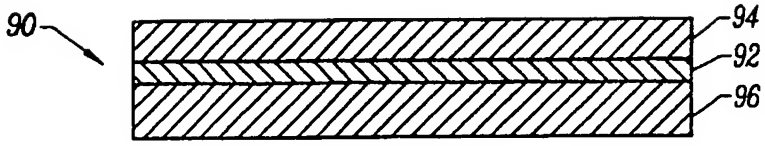

FIG. 9a

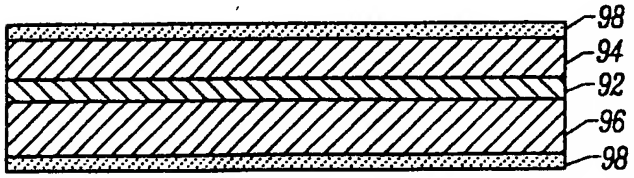

FIG. 9b

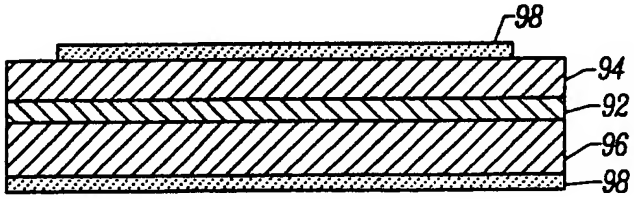

FIG. 9c

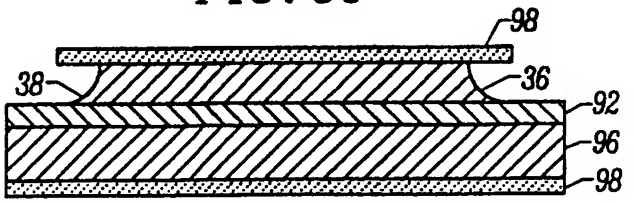

FIG. 9d

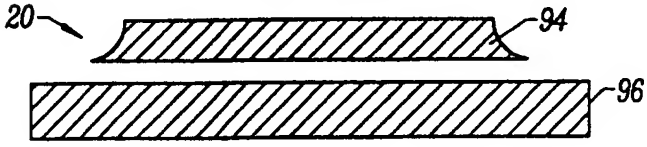

FIG. 9e

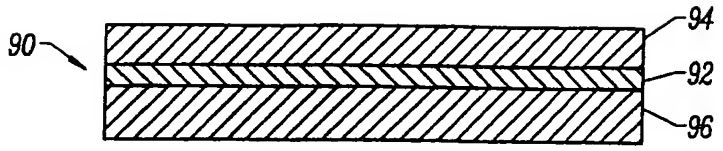

FIG. 10a

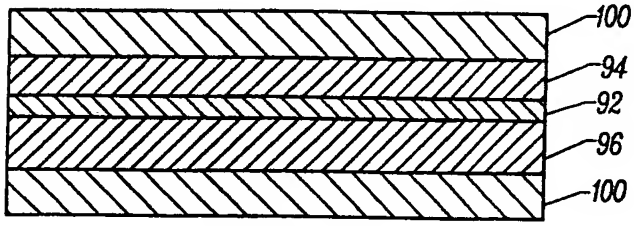

FIG. 10b

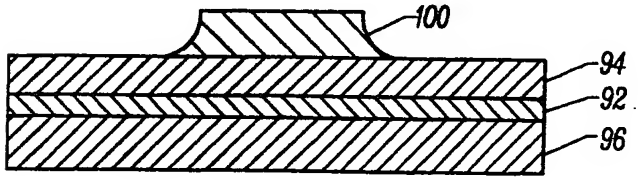

FIG. 10c

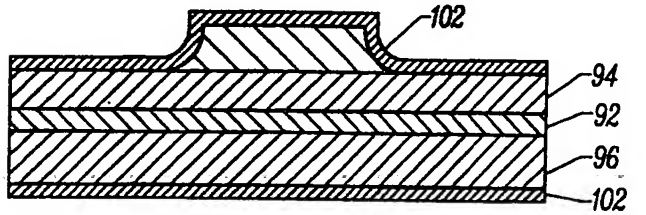

FIG. 10d

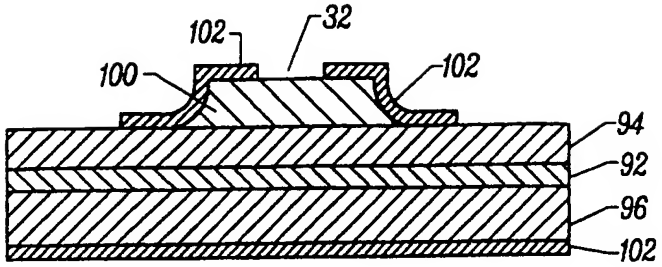

FIG. 10e

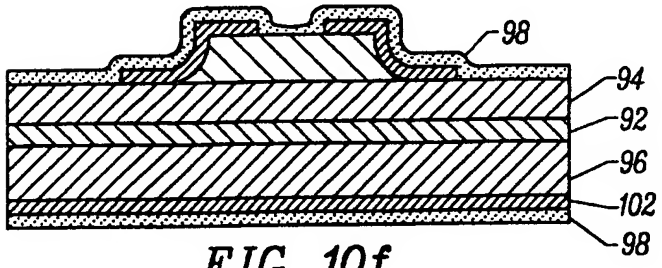

FIG. 10f

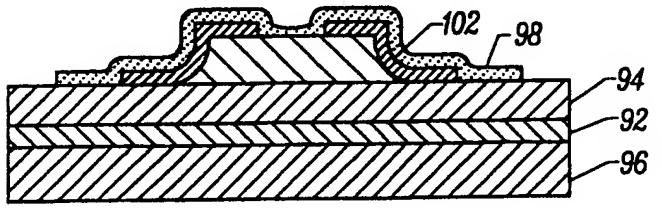

FIG. 10g

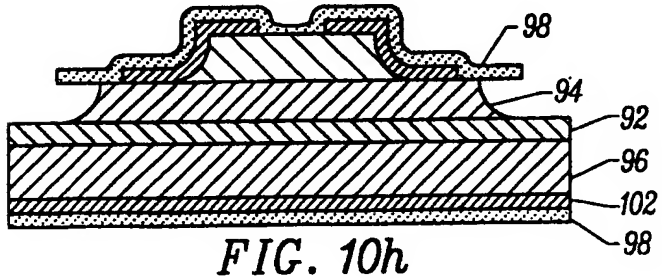

FIG. 10h

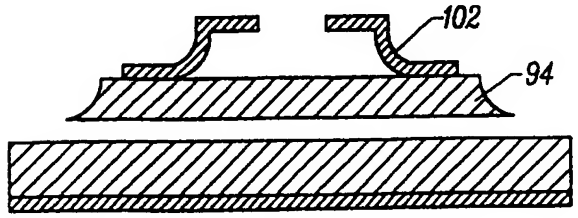

FIG. 10i

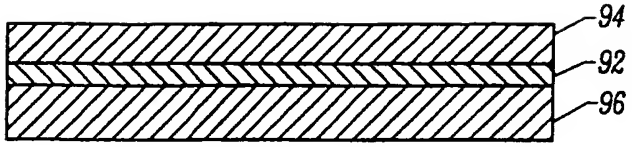

FIG. 11a

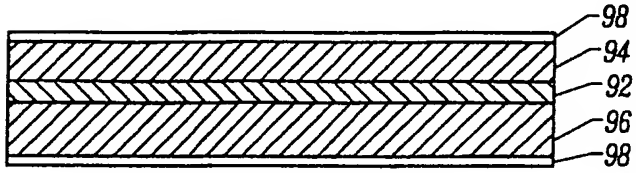

FIG. 11b

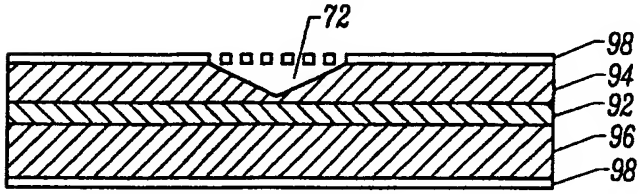

FIG. 11c

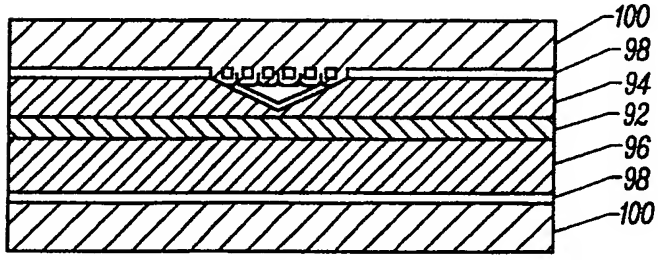

FIG. 11d

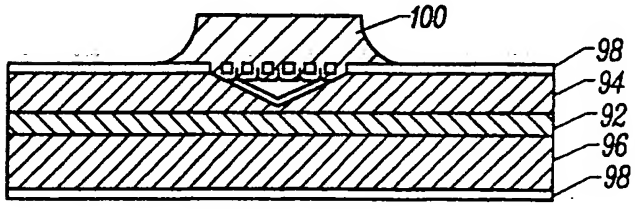

FIG. 11e

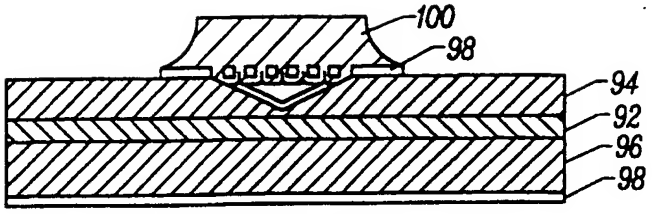

FIG. 11f

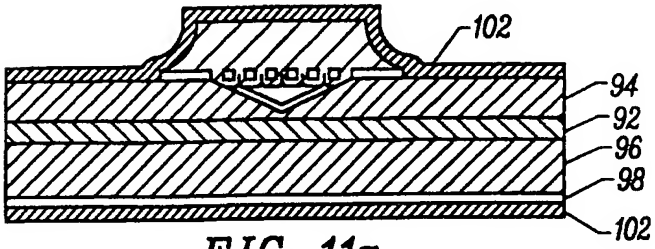

FIG. 11g

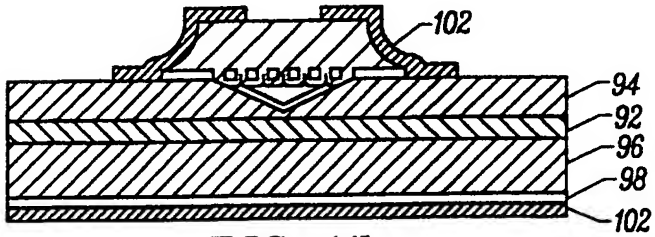

FIG. 11h

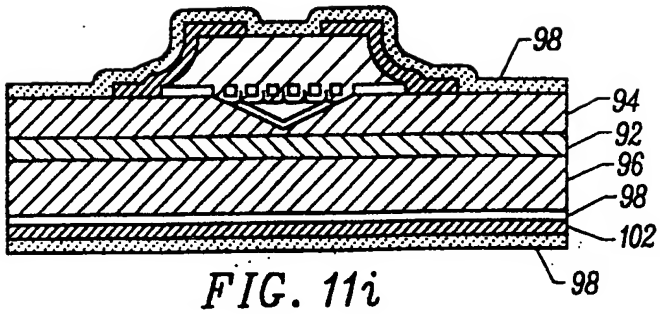

FIG. 11i

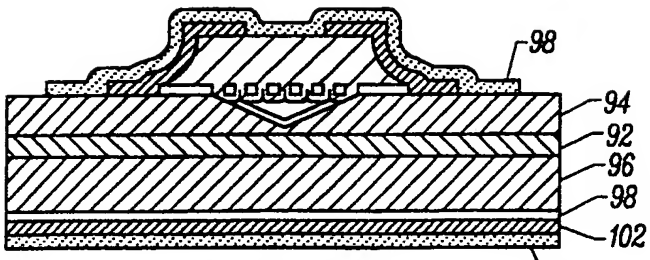

FIG. 11j

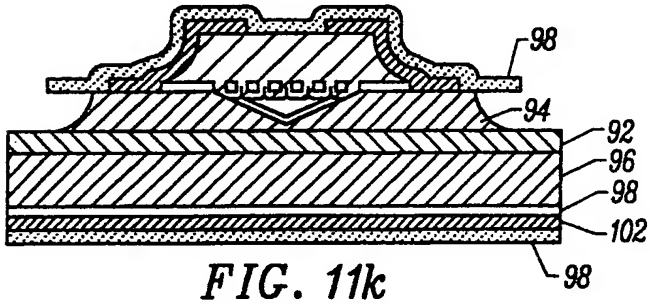

FIG. 11k

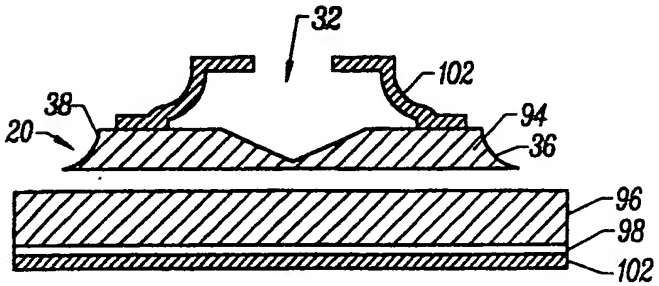

FIG. 11l

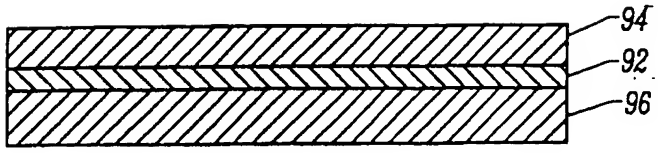

FIG. 12a

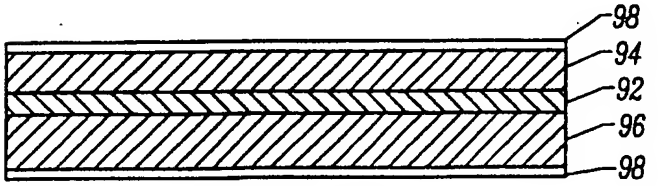

FIG. 12b

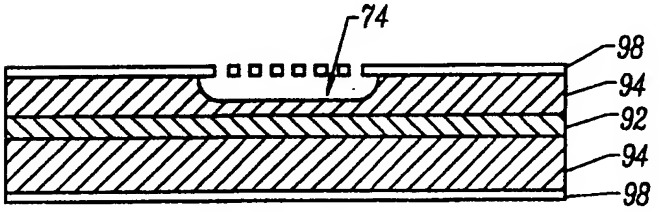

FIG. 12c

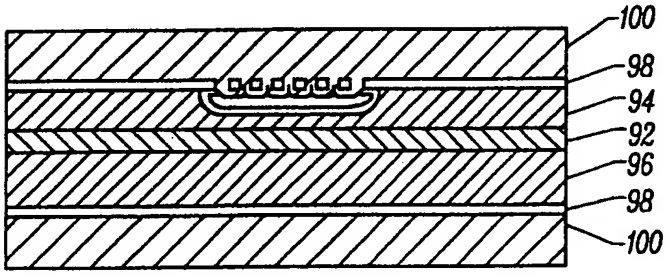

FIG. 12d

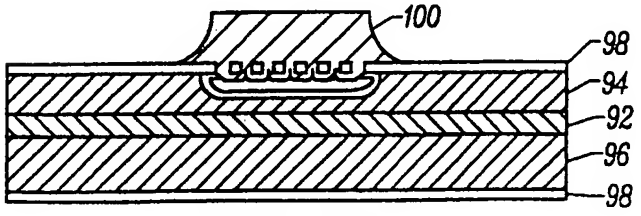

FIG. 12e

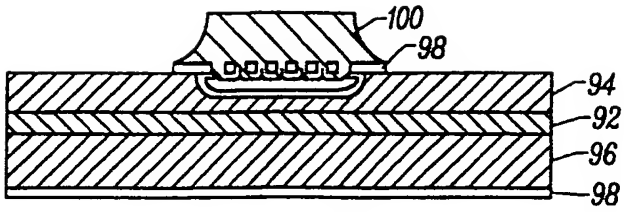

FIG. 12f

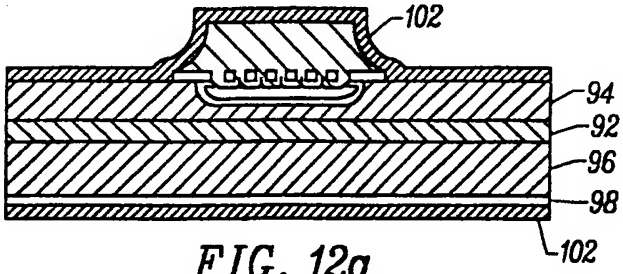

FIG. 12g

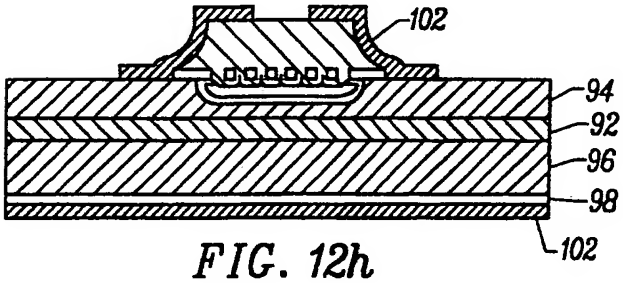

FIG. 12h

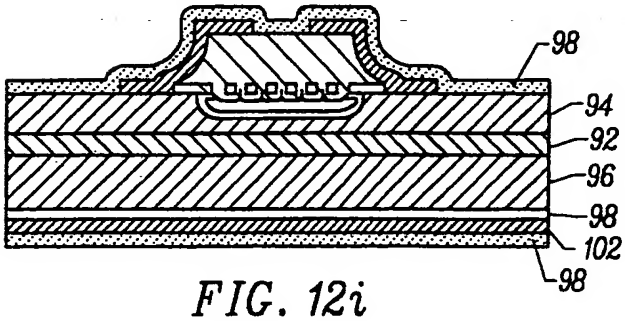

FIG. 12i

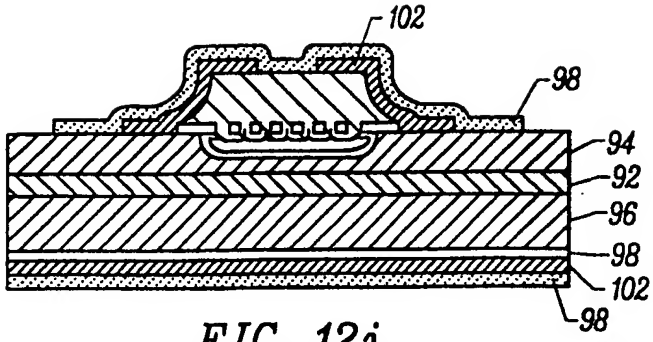

FIG. 12j

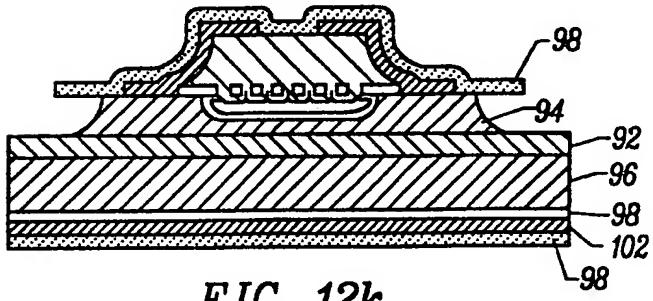

FIG. 12k

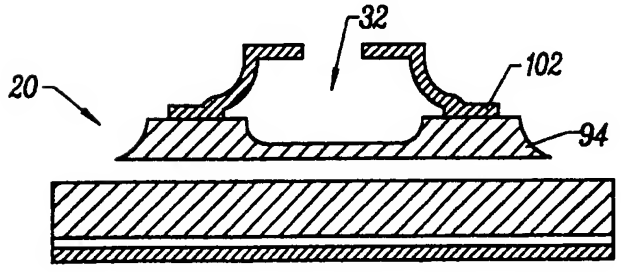

FIG. 12l

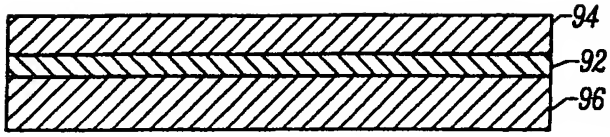

FIG. 13a

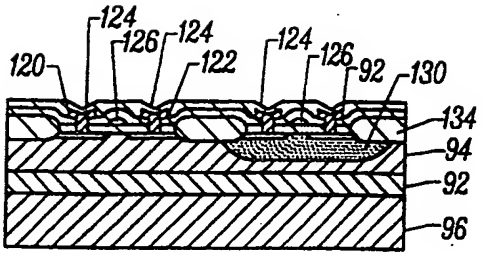

FIG. 13a'

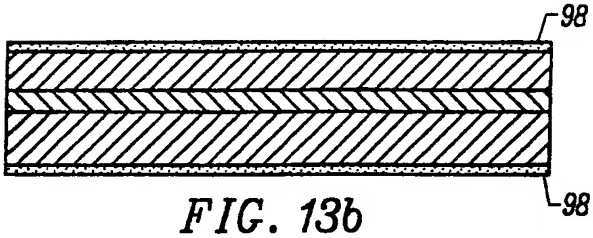

FIG. 13b

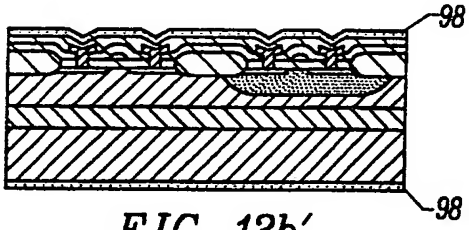

FIG. 13b'

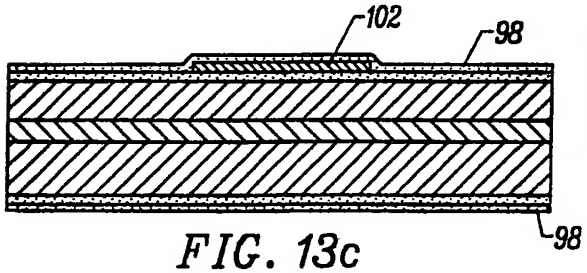

FIG. 13c

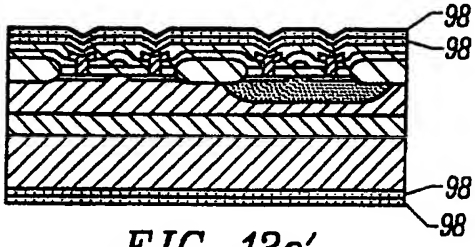

FIG. 13c'

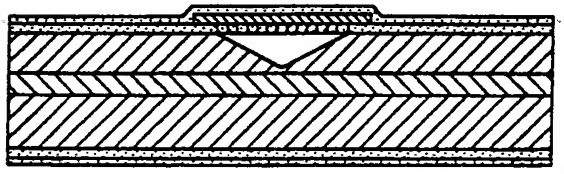

FIG. 13d

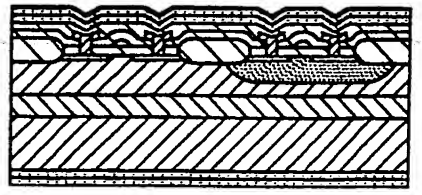

FIG. 13d'

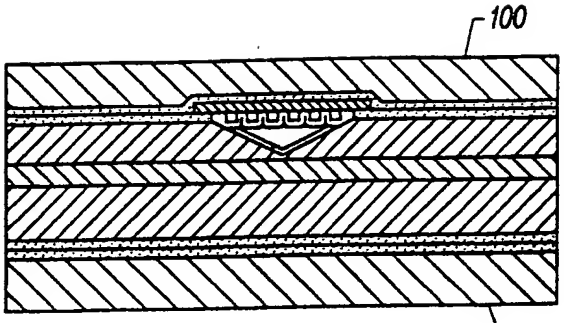

FIG. 13e

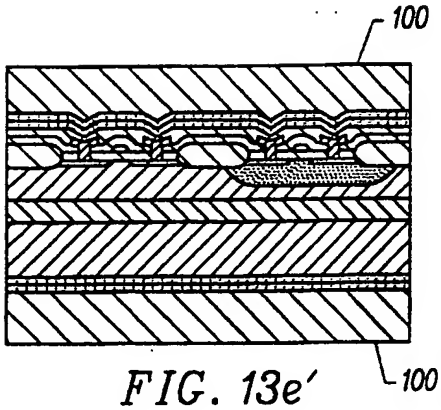

FIG. 13e'

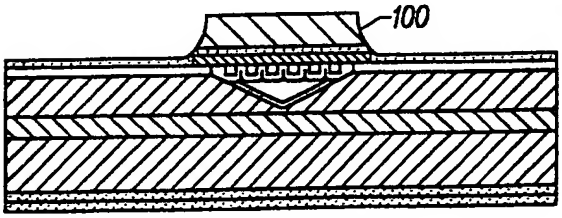

FIG. 13f

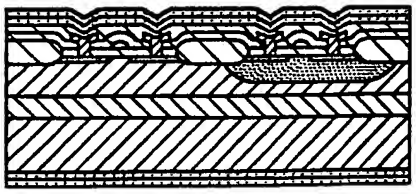

FIG. 13f'

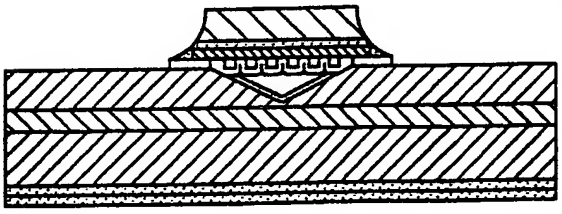

FIG. 13g

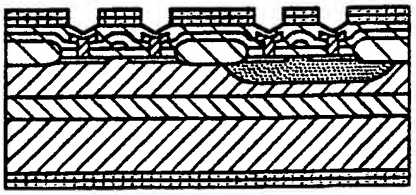

FIG. 13g'

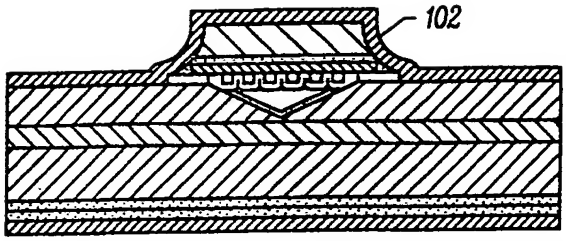

FIG. 13h

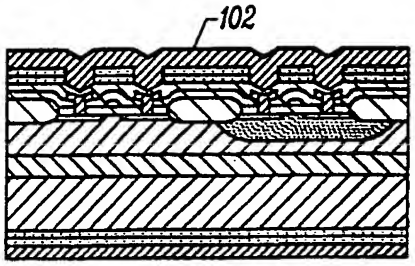

FIG. 13h'

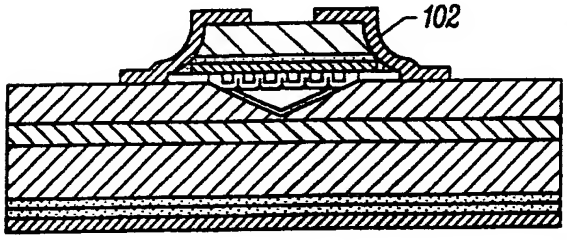

FIG. 13i

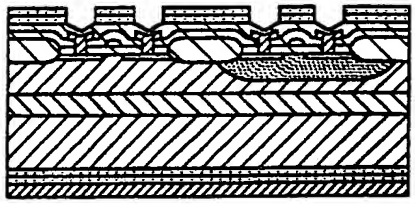

FIG. 13i'

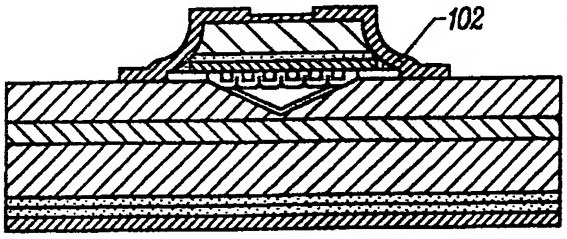

FIG. 13j

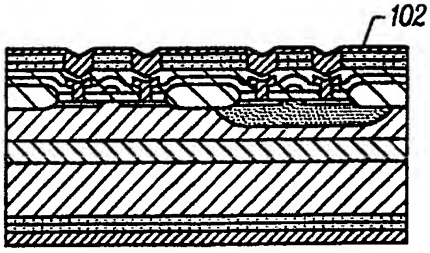

FIG. 13j'

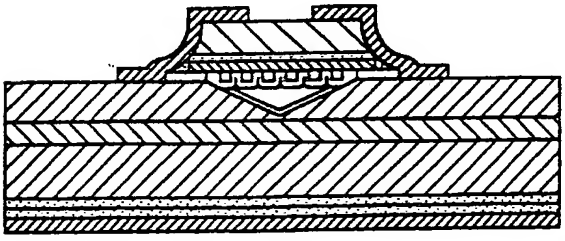

FIG. 13k

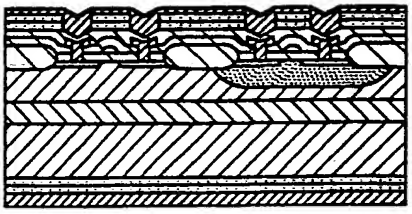

FIG. 13k'

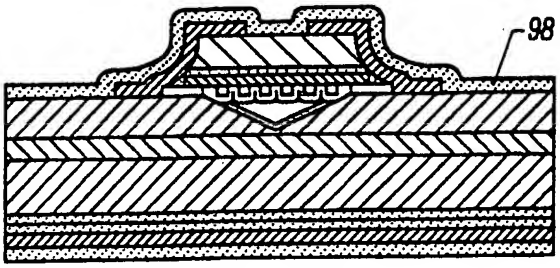

FIG. 13l

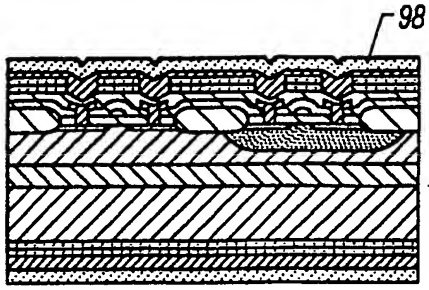

FIG. 13l'

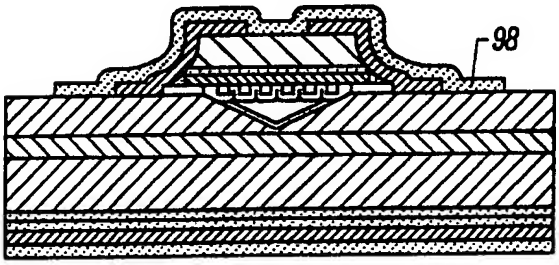

FIG. 13m

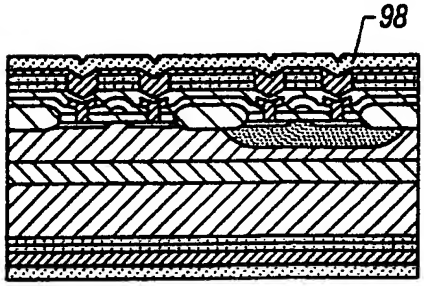

FIG. 13m'

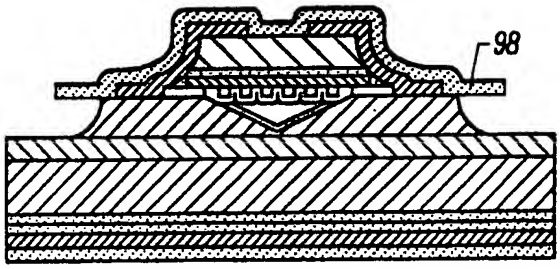

FIG. 13n

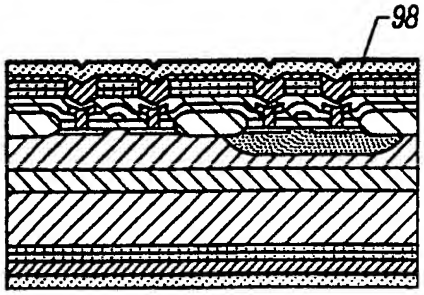

FIG. 13n'

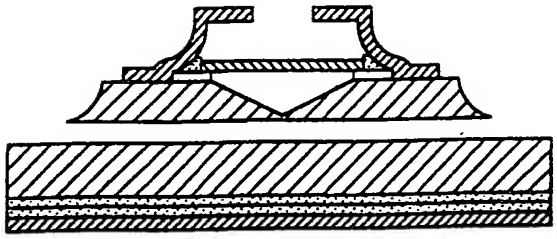

FIG. 13o

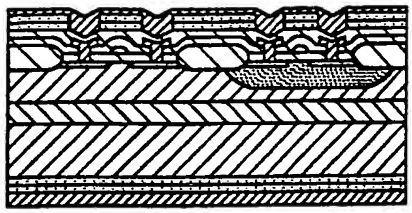

FIG. 13o'

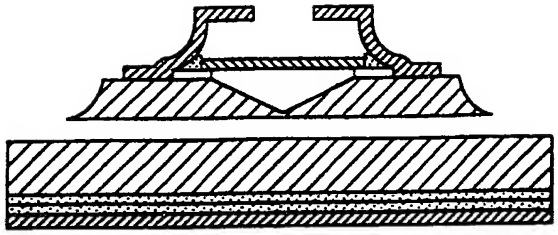

FIG. 13p

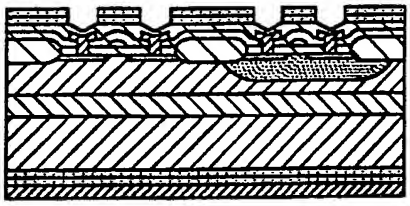

FIG. 13p'

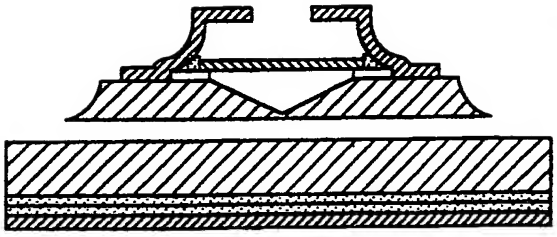

FIG. 13q

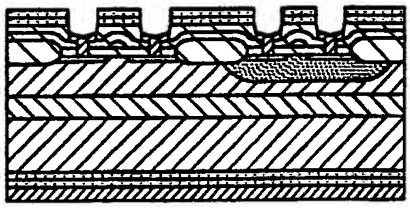

FIG. 13q'

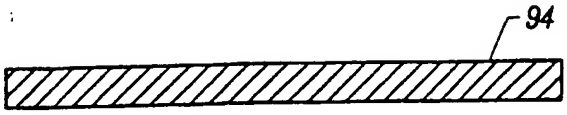

FIG. 14a

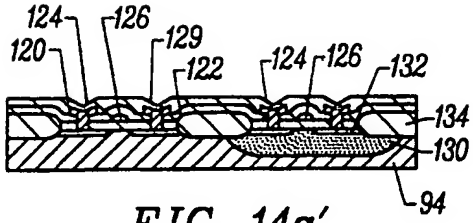

FIG. 14a'

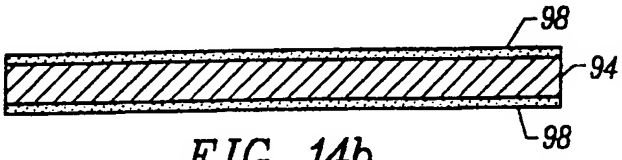

FIG. 14b

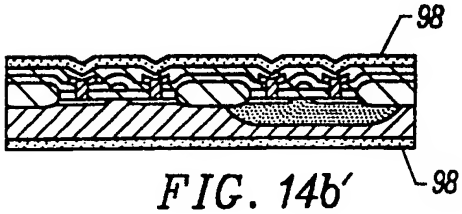

FIG. 14b'

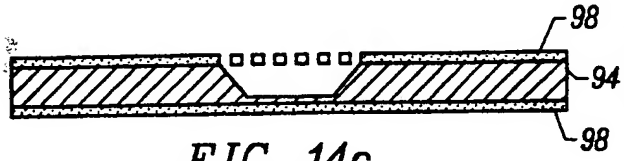

FIG. 14c

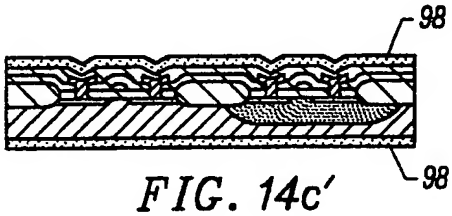

FIG. 14c'

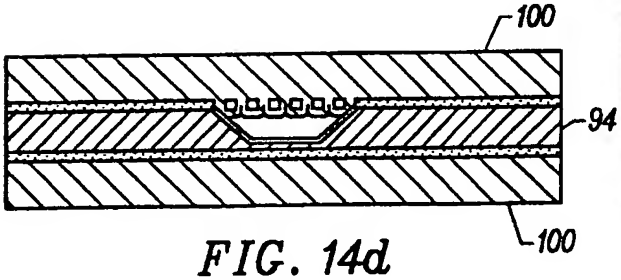

FIG. 14d

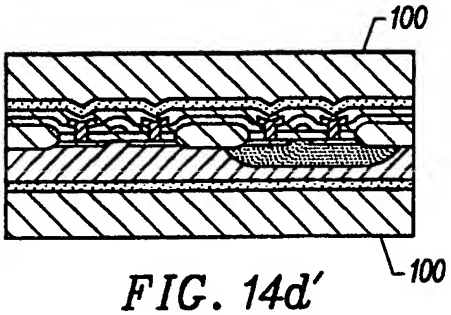

FIG. 14d'

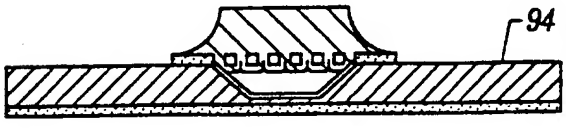

FIG. 14e

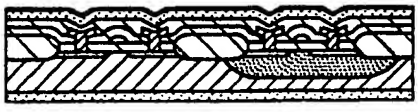

FIG. 14e'

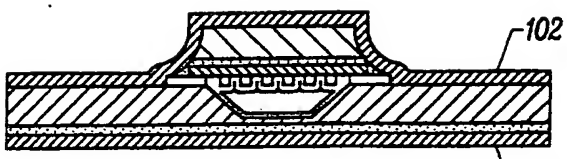

FIG. 14f

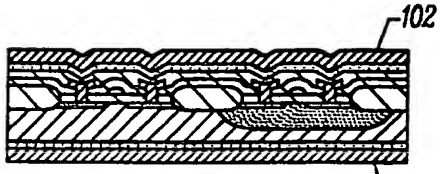

FIG. 14f'

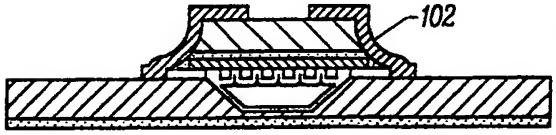

FIG. 14g

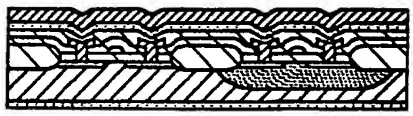

FIG. 14g'

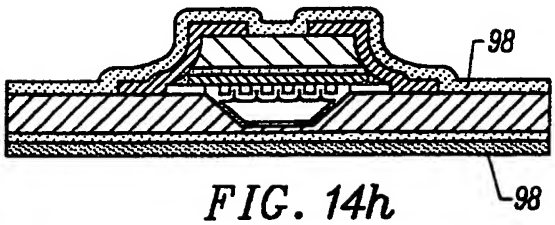

FIG. 14h

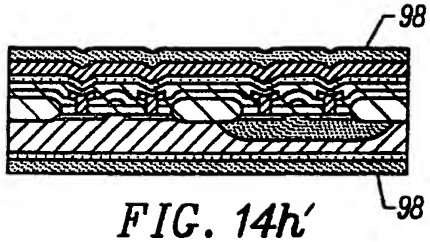

FIG. 14h'

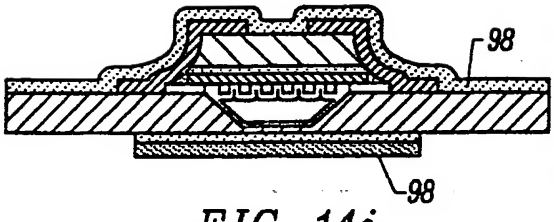

FIG. 14i

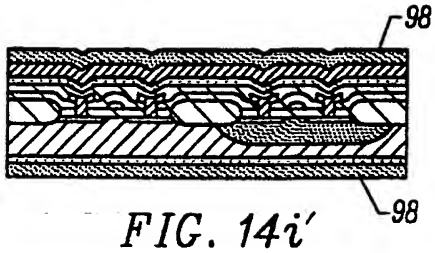

FIG. 14i'

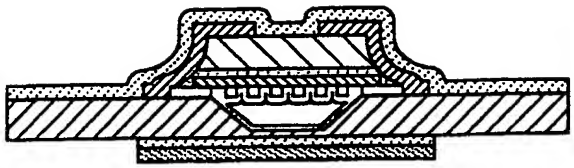

FIG. 14j

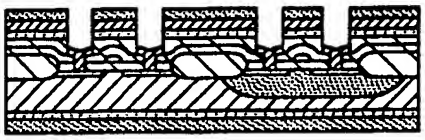

FIG. 14j'

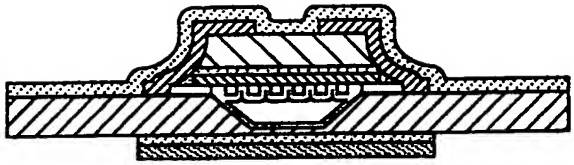

FIG. 14k

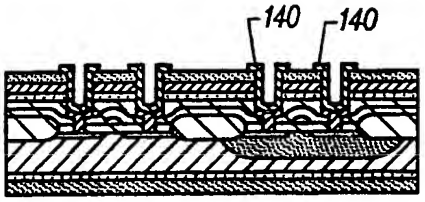

FIG. 14k'

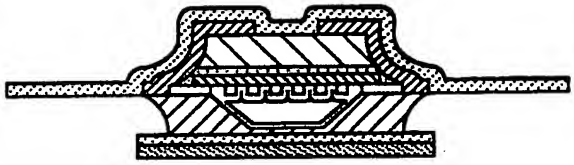

FIG. 14l

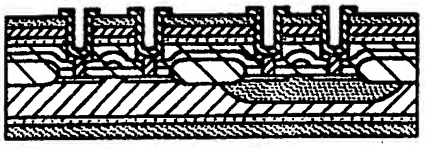

FIG. 14l'

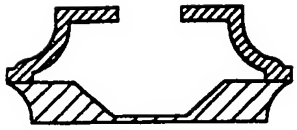

FIG. 14m

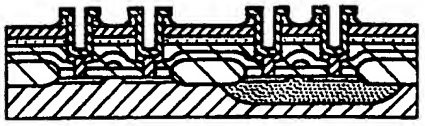

FIG. 14m'

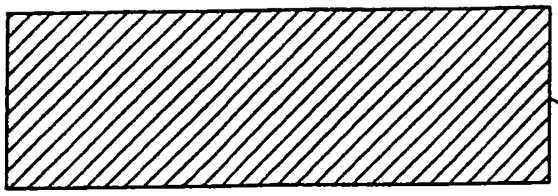

FIG. 15a

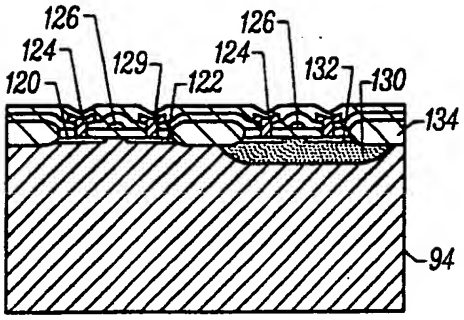

FIG. 15a'

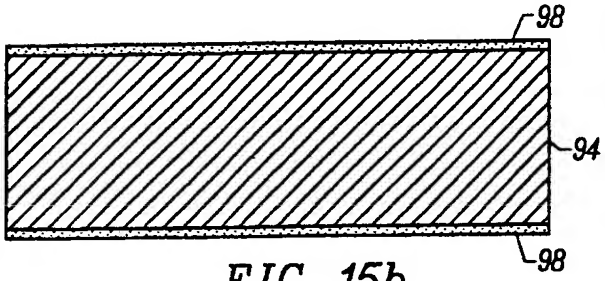

FIG. 15b

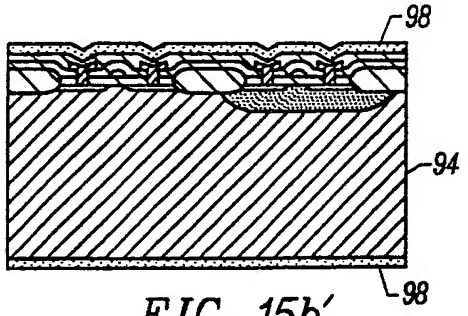

FIG. 15b'

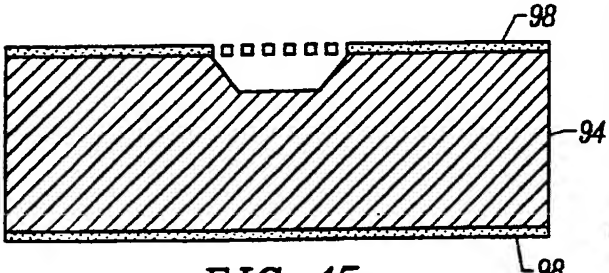

FIG. 15c

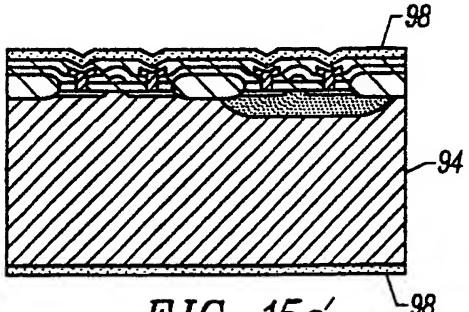

FIG. 15c'

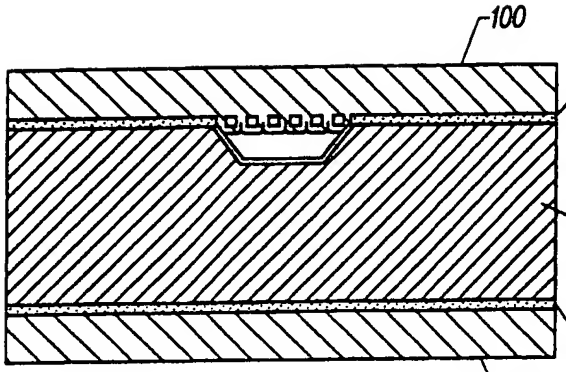

FIG. 15d

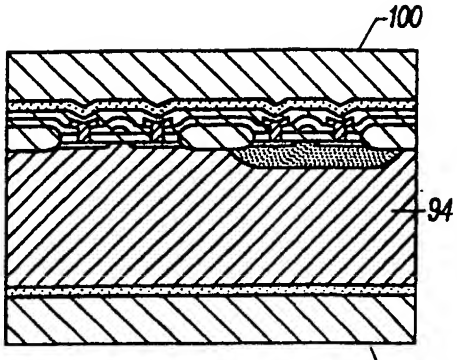

FIG. 15d'

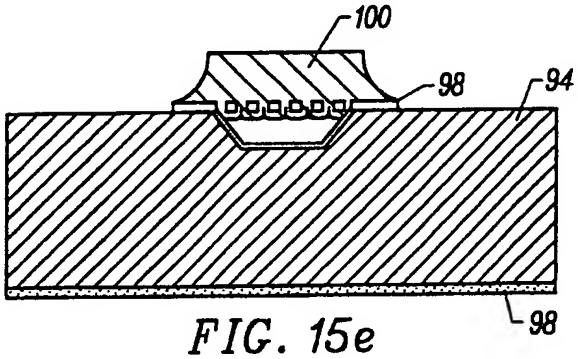

FIG. 15e

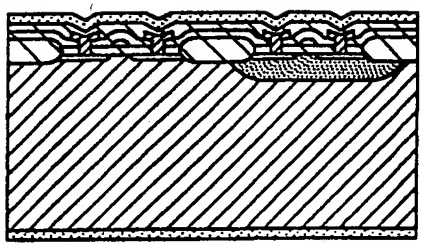

FIG. 15e'

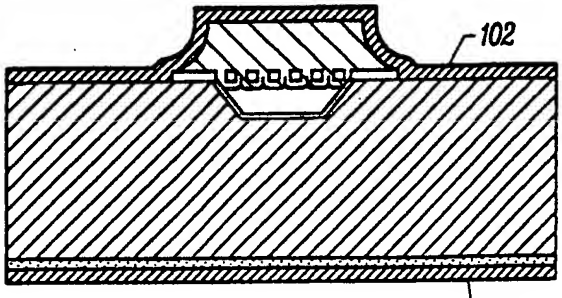

FIG. 15f

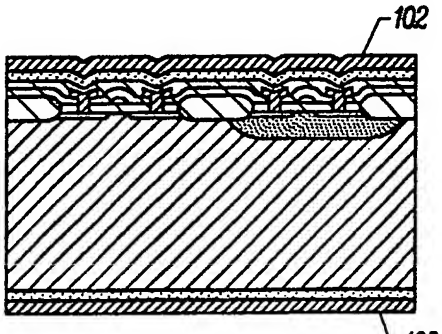

FIG. 15f'

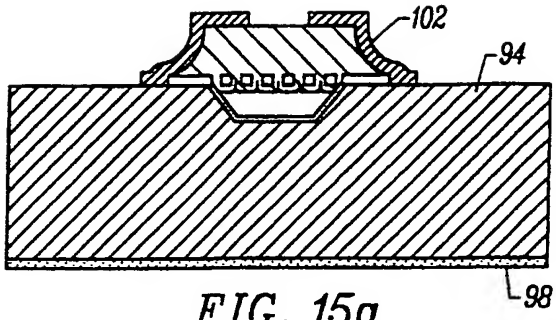

FIG. 15g

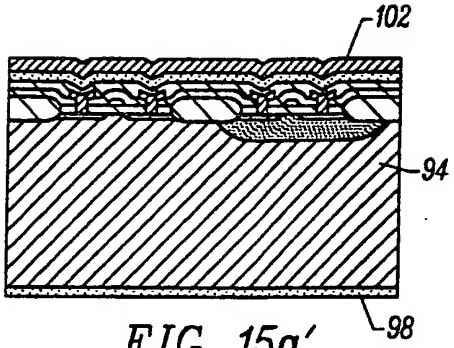

FIG. 15g'

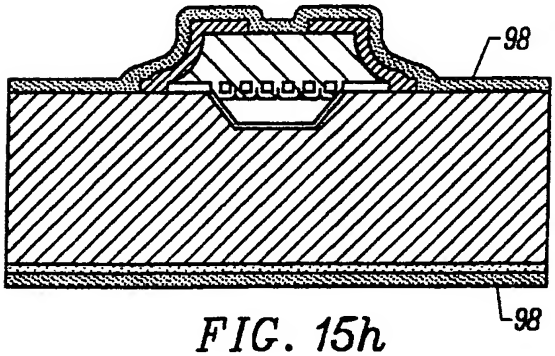

FIG. 15h

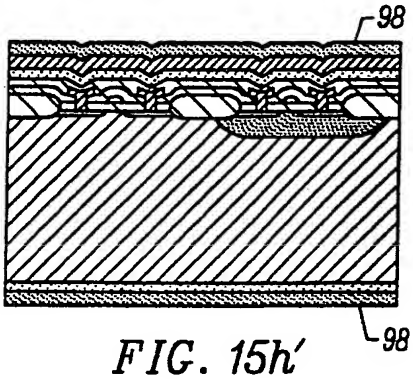

FIG. 15h'

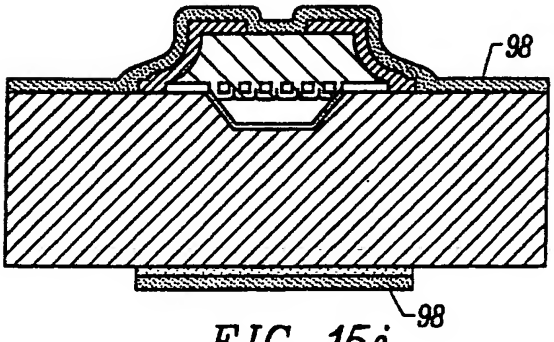

FIG. 15i

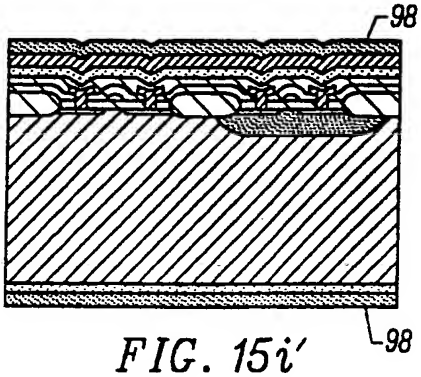

FIG. 15i'

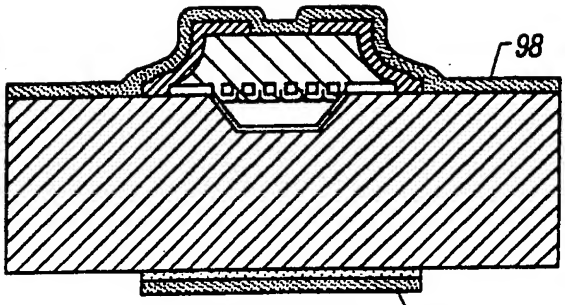

FIG. 15j

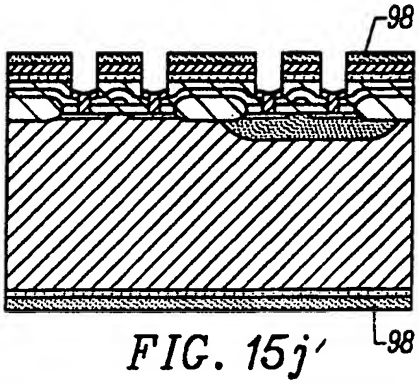

FIG. 15j'

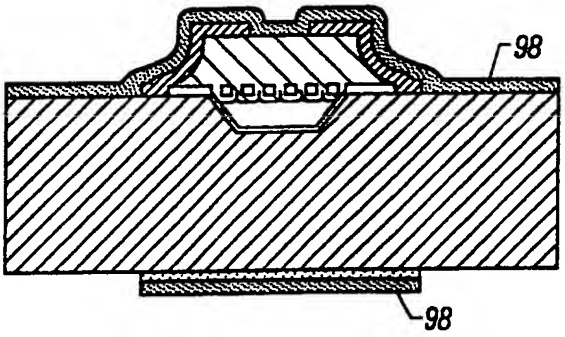

FIG. 15k

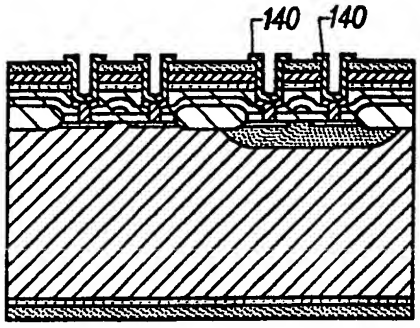

FIG. 15k'

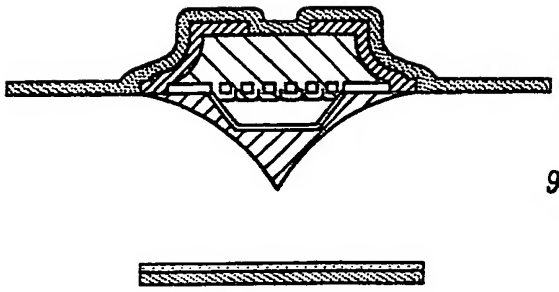

FIG. 15l

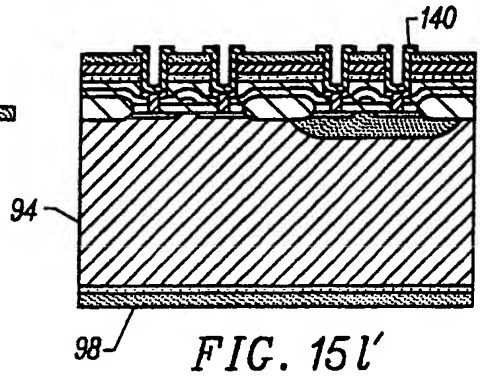

FIG. 15l'

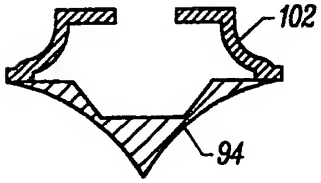

FIG. 15m

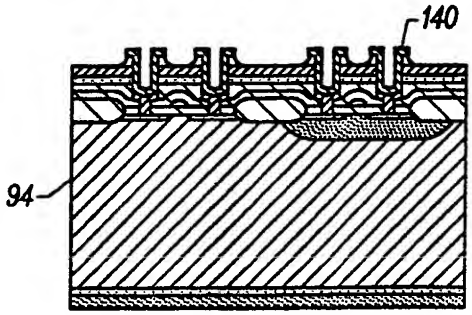

FIG. 15m'

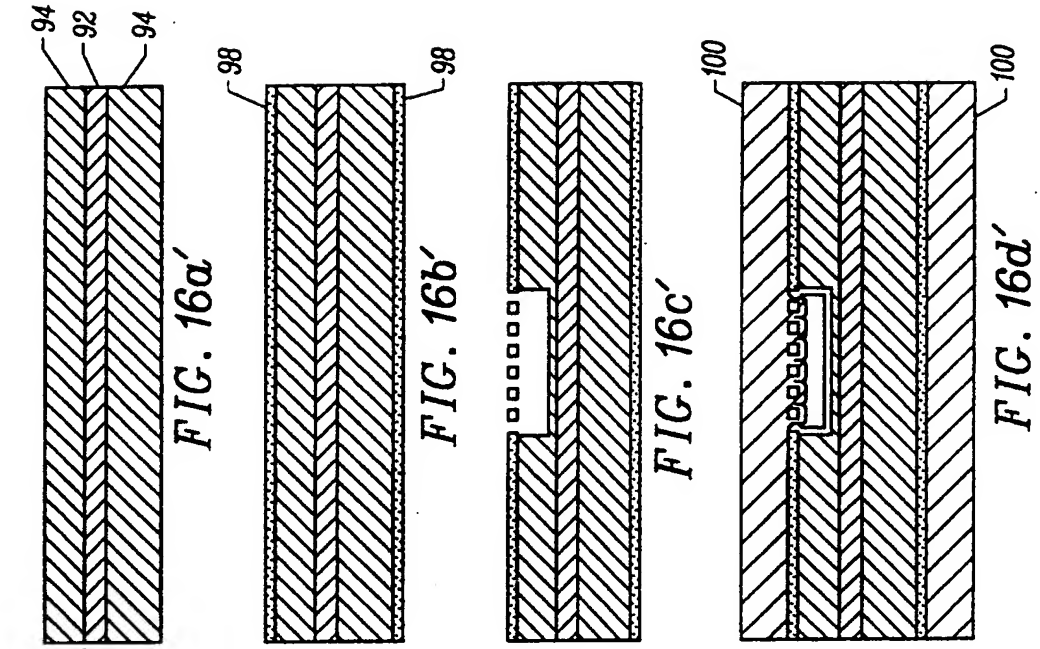

FIG. 16a' FIG. 16b' FIG. 16c' FIG. 16d'

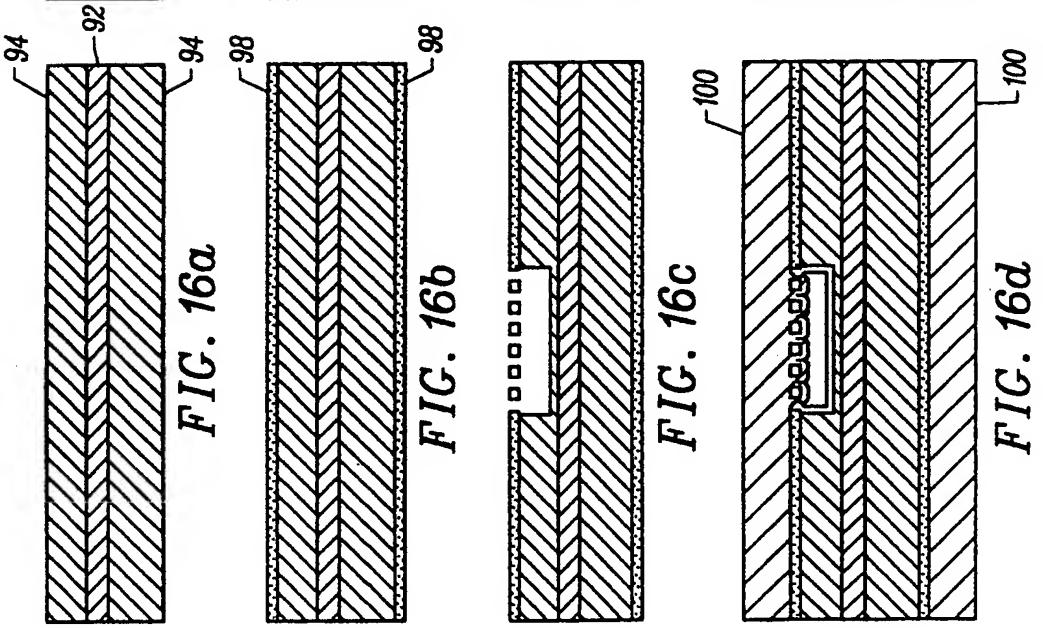

FIG. 16a FIG. 16b FIG. 16c FIG. 16d

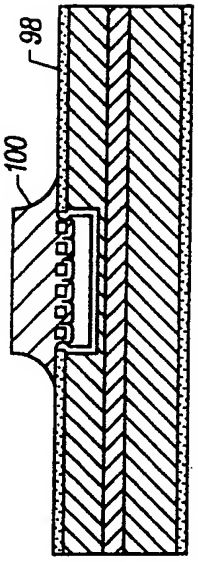

FIG. 16e'

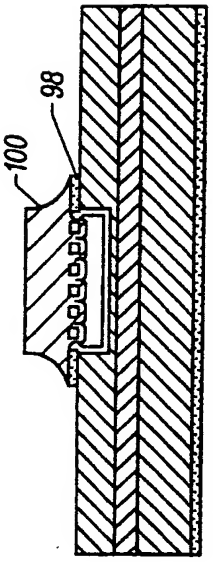

FIG. 16f'

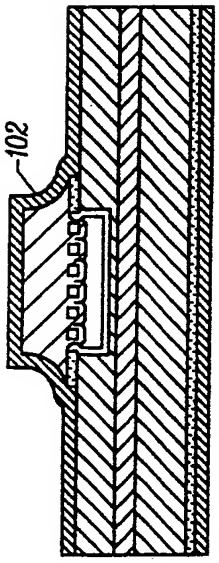

FIG. 16g'

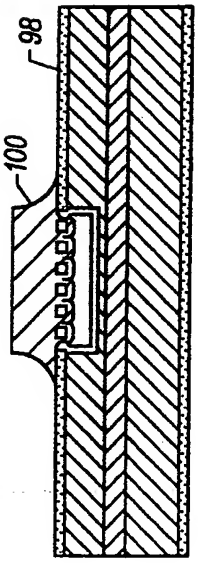

FIG. 16e

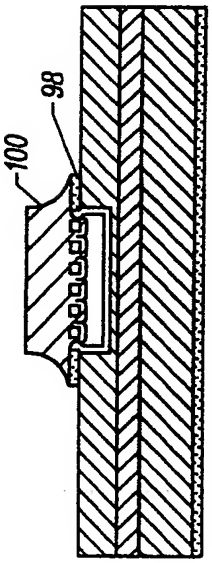

FIG. 16f

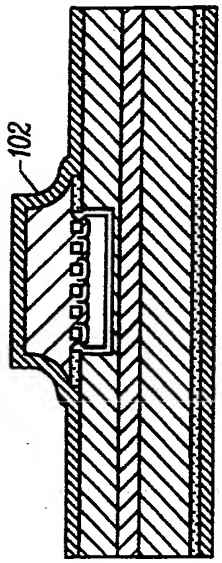

FIG. 16g

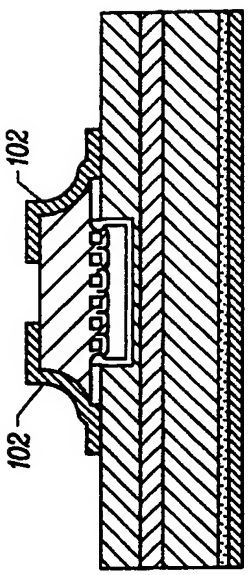

FIG. 16h'

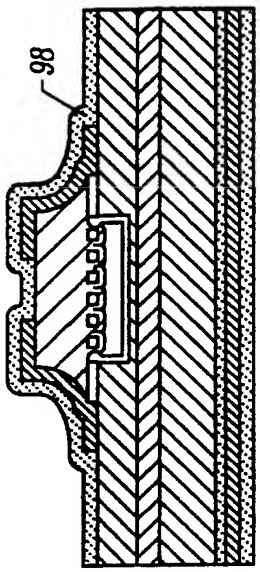

FIG. 16i'

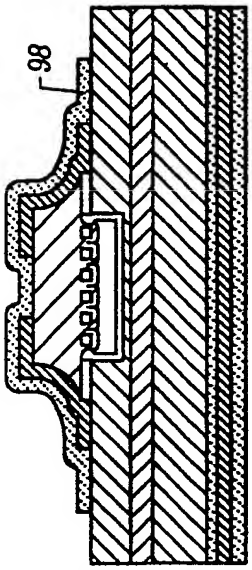

FIG. 16j'

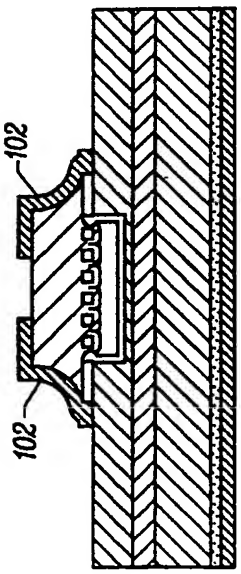

FIG. 16h

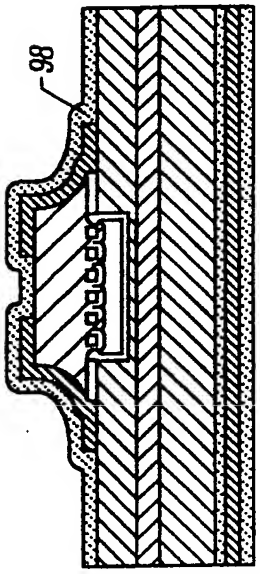

FIG. 16i

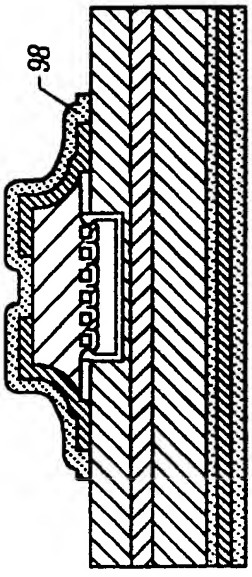

FIG. 16j

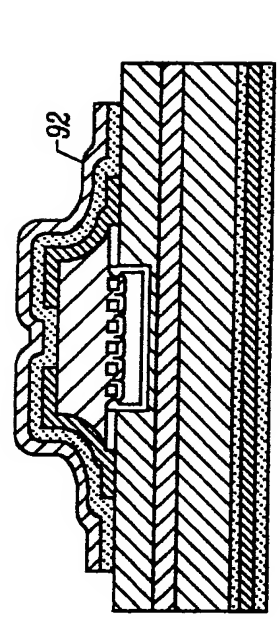

FIG. 16k'

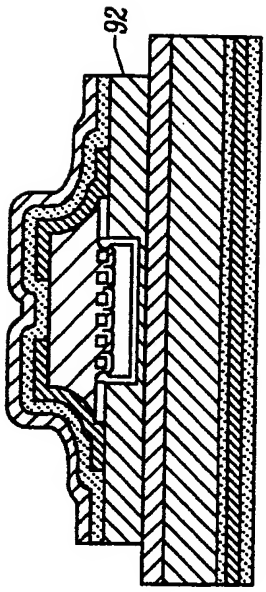

FIG. 16l'

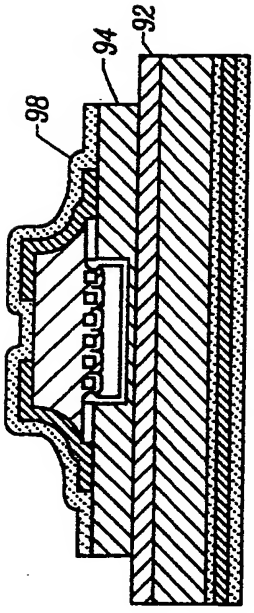

FIG. 16m'

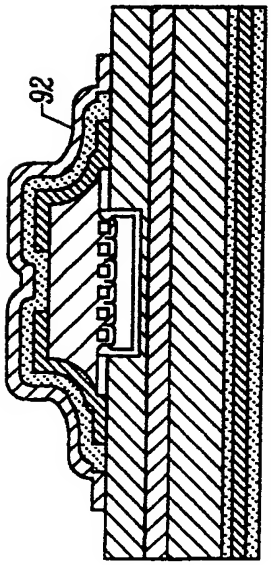

FIG. 16k

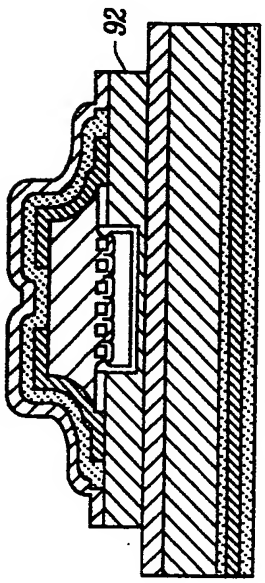

FIG. 16l

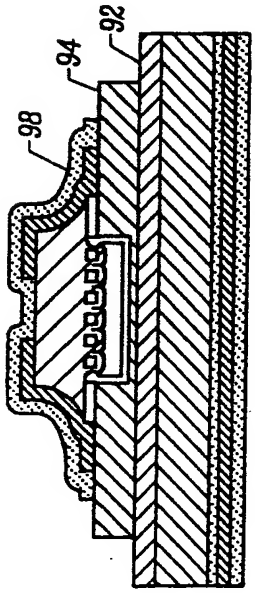

FIG. 16m

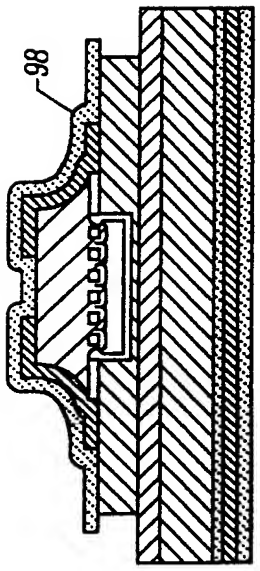

FIG. 16n'

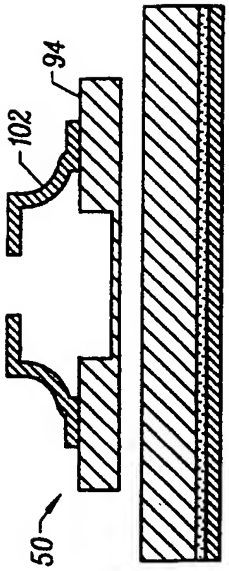

FIG. 16o'

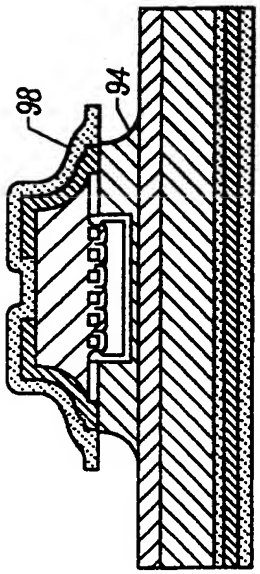

FIG. 16n

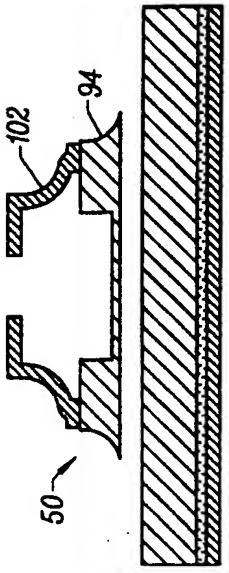

FIG. 16o

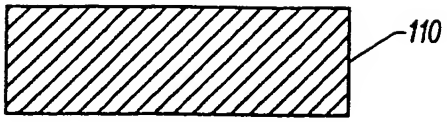

FIG. 17a

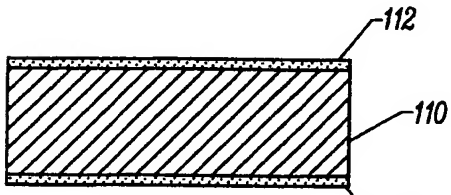

FIG. 17b

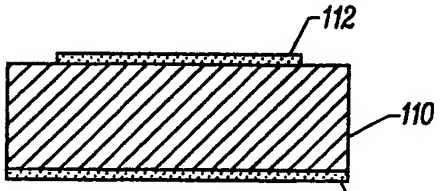

FIG. 17c

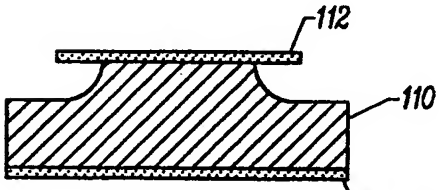

FIG. 17d

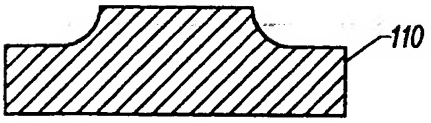

FIG. 17e

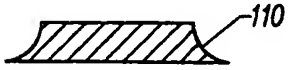

FIG. 17f

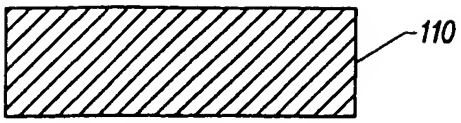

FIG. 18a

FIG. 18b

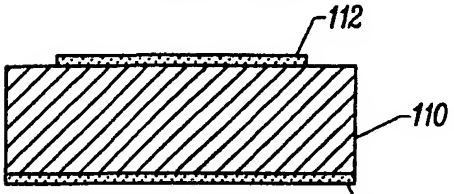

FIG. 18c

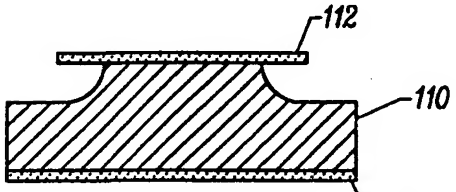

FIG. 18d

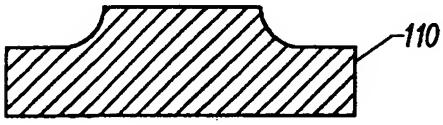

FIG. 18e

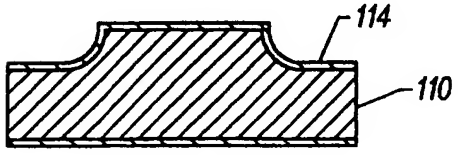

FIG. 18f

FIG. 17g

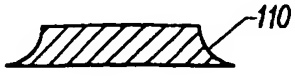

FIG. 18h

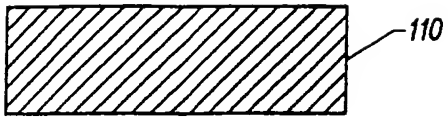

FIG. 19a

FIG. 19b

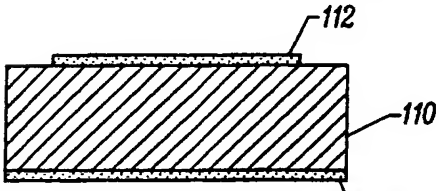

FIG. 19c

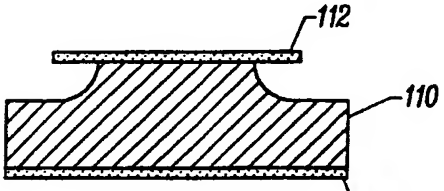

FIG. 19d

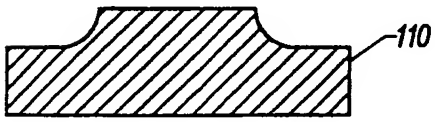

FIG. 19e

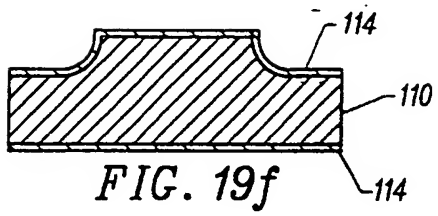

FIG. 19f

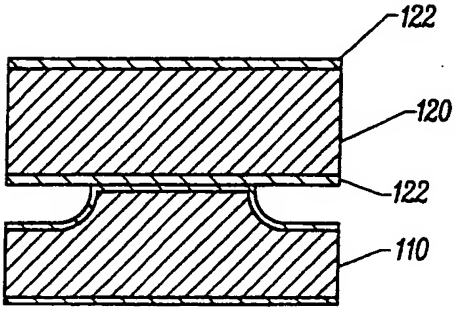

FIG. 19g

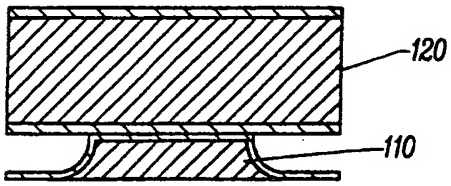

FIG. 19h

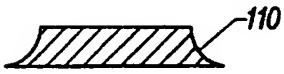

FIG. 19i

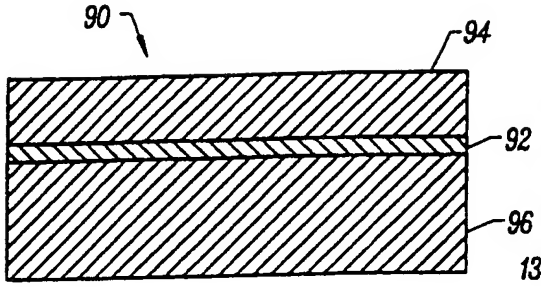

FIG. 20g

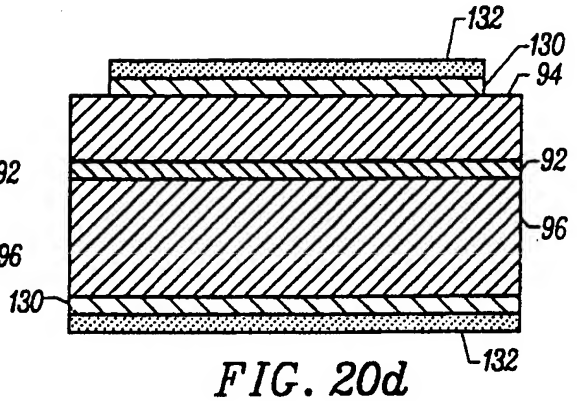

FIG. 20d

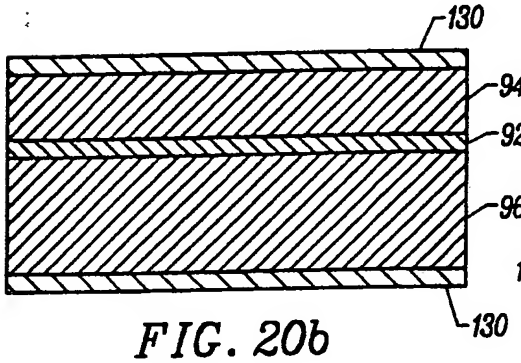

FIG. 20b

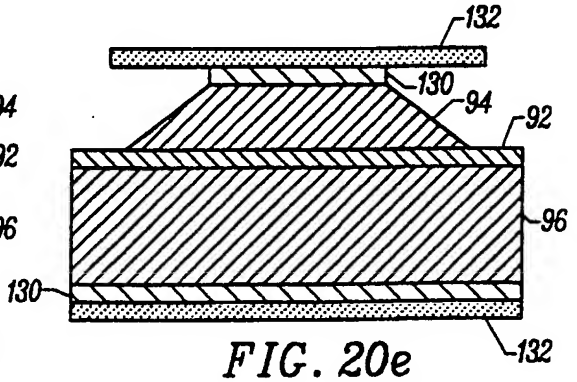

FIG. 20e

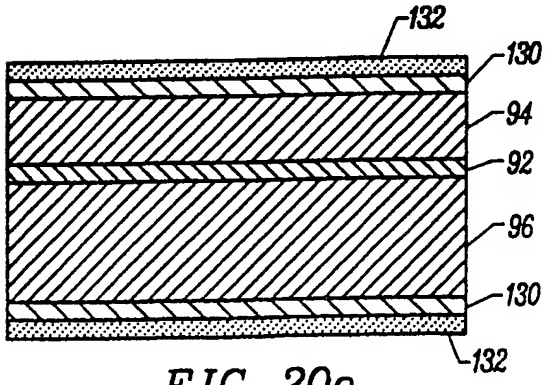

FIG. 20c

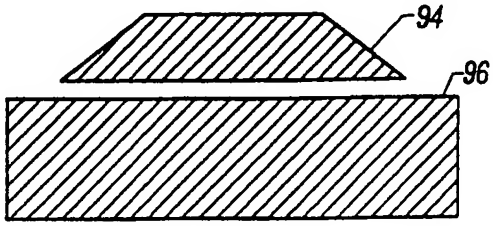

FIG. 20f

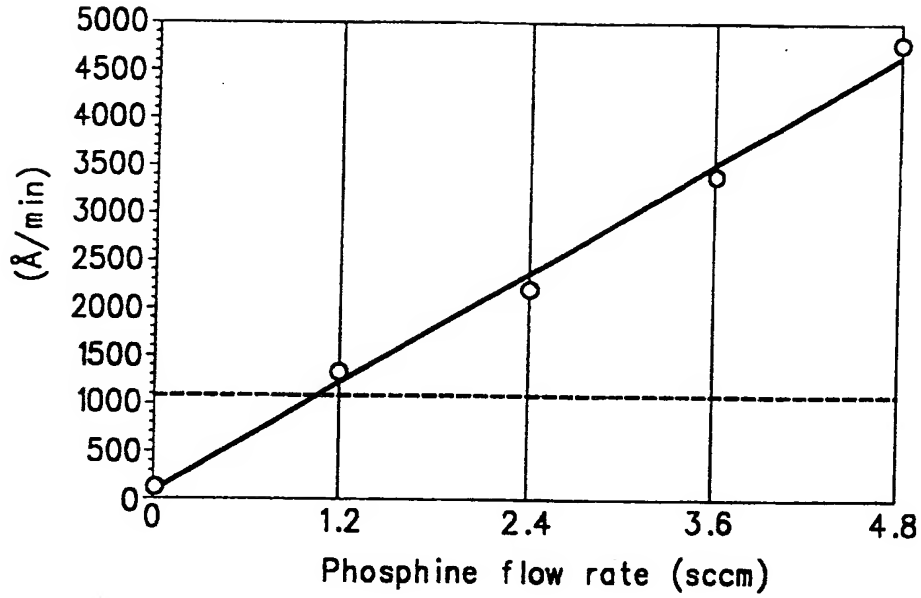
5000
4500
4000
3500
3000
2500
2000
1500
1000
500
0
(Å/min)
0
1.2
2.4
3.6
4.8
Phosphine flow rate (sccm)

FIG. 21

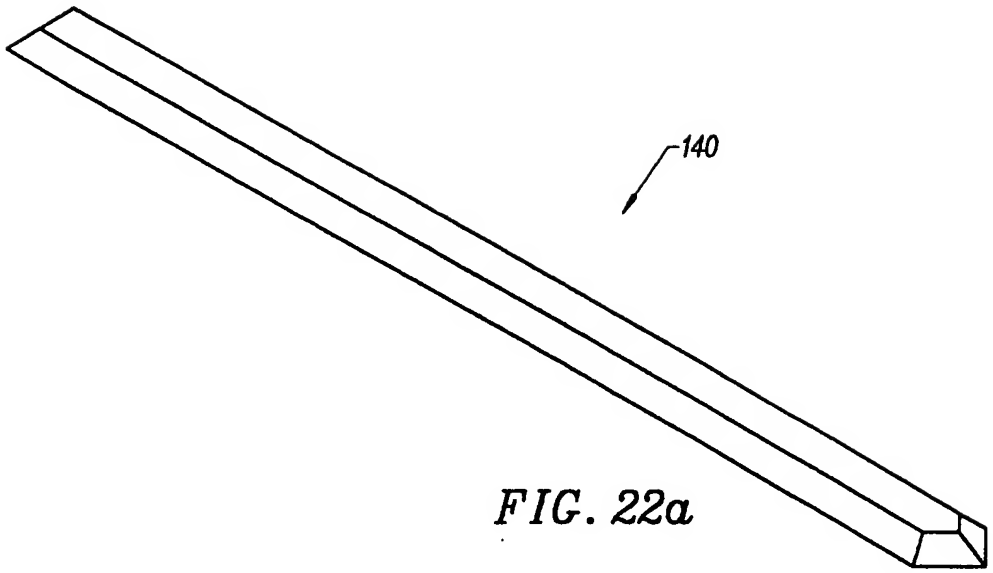

FIG. 22a

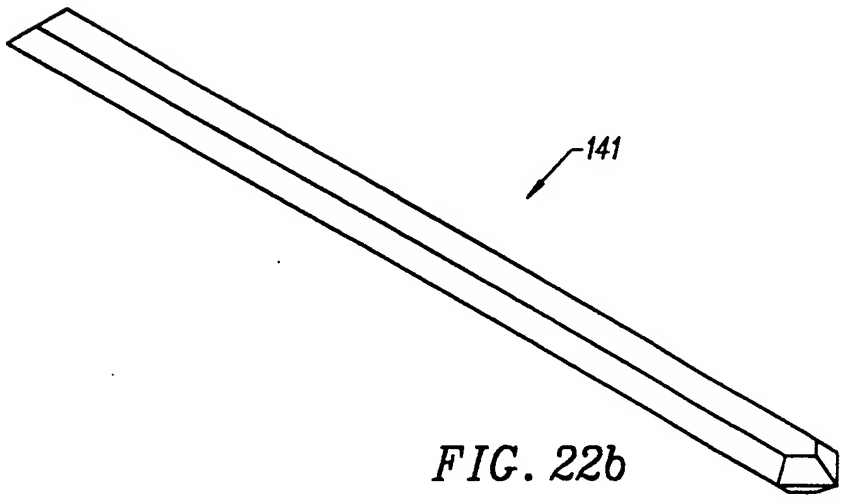

FIG. 22b

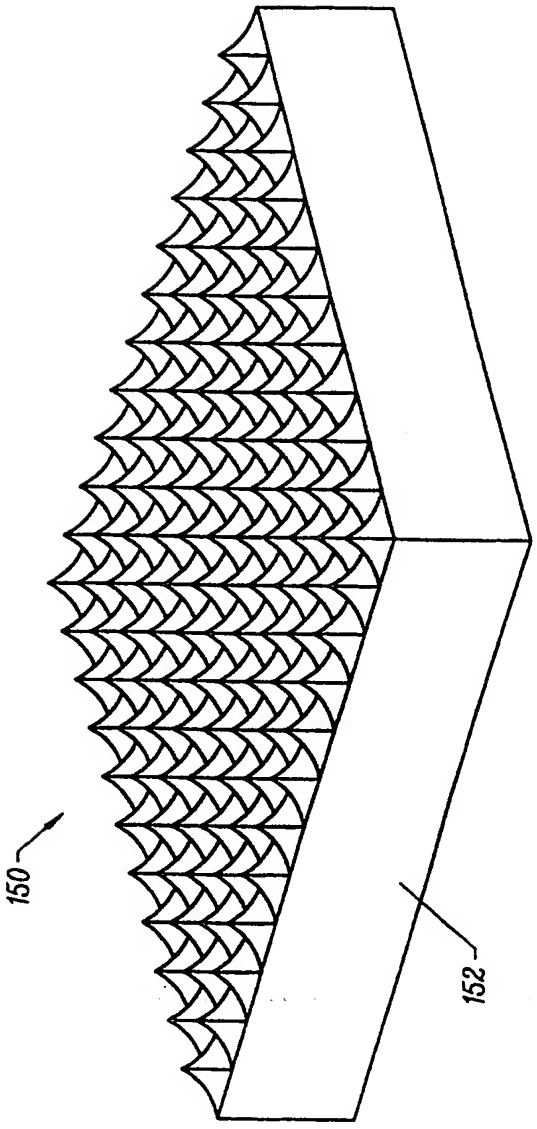

FIG. 23

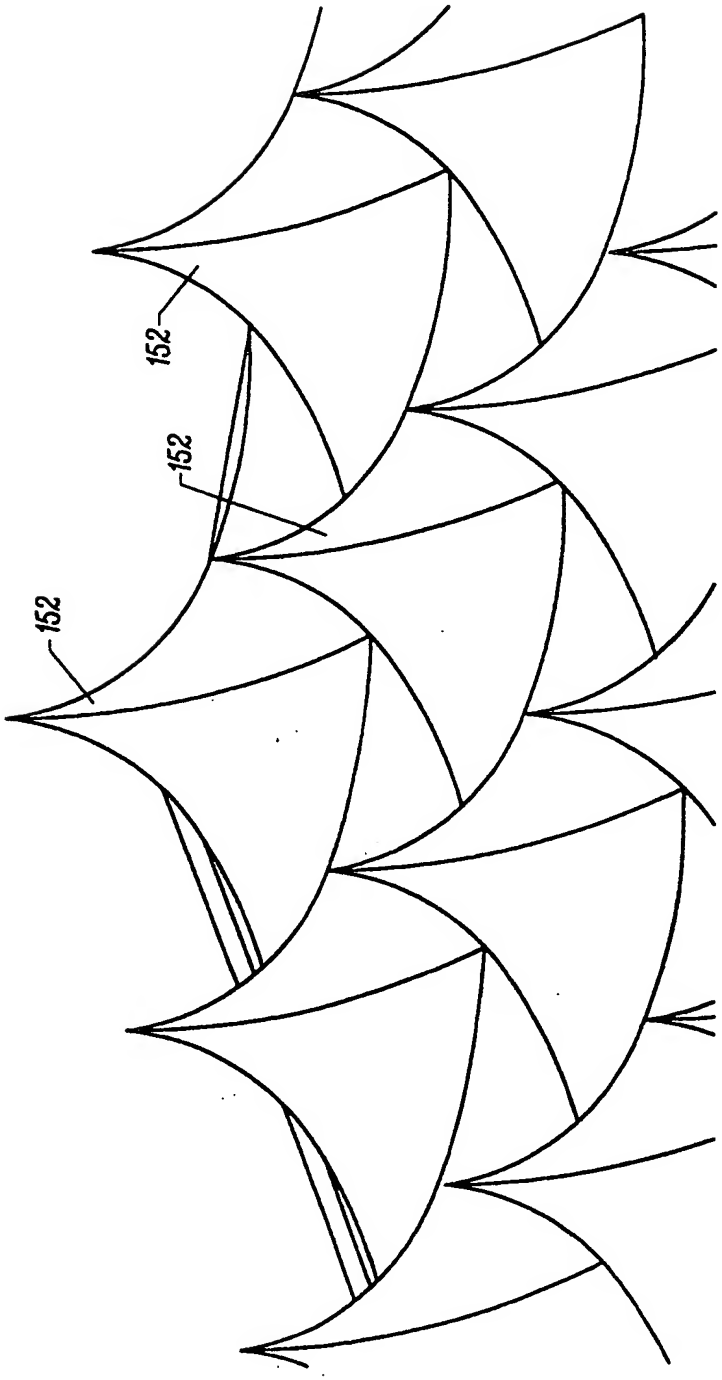

FIG. 24

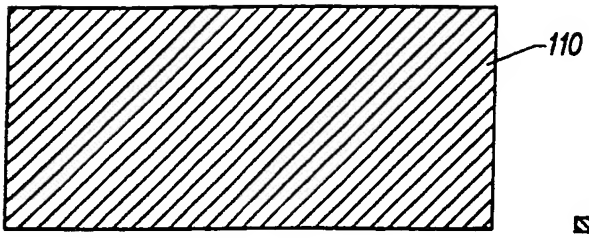

FIG. 25a

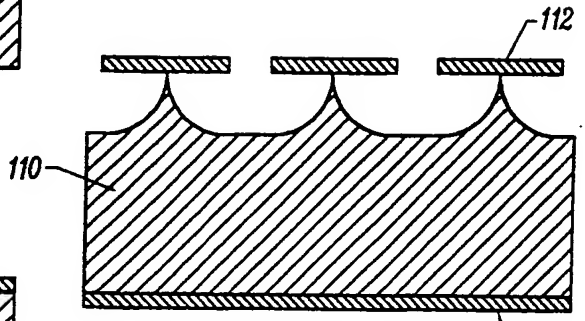

FIG. 25d

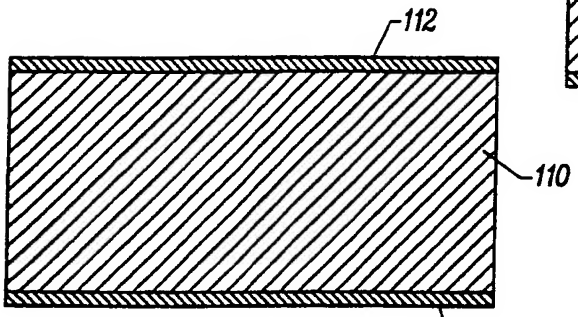

FIG. 25b

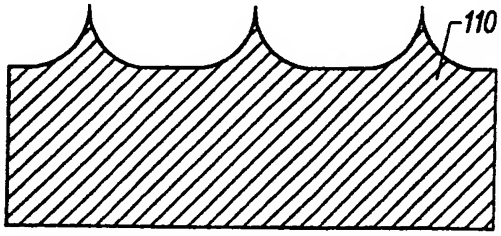

FIG. 25e

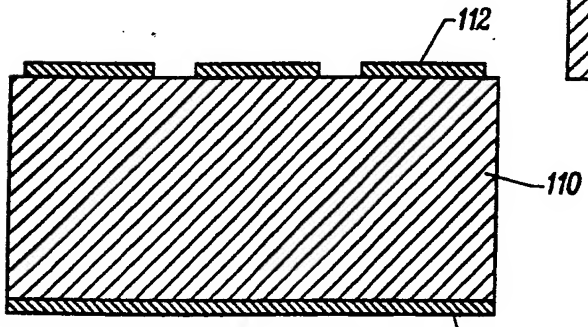

FIG. 25c

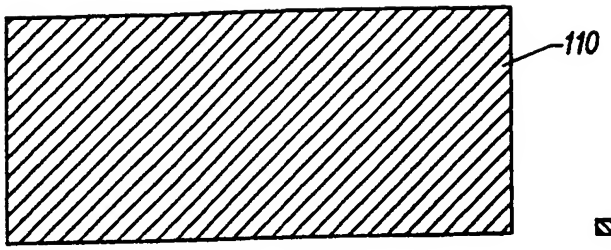

FIG. 26a

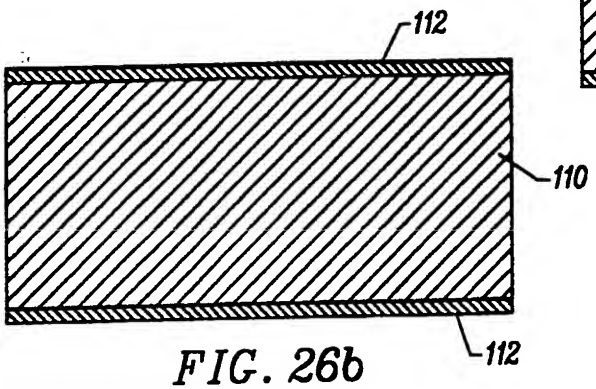

FIG. 26b

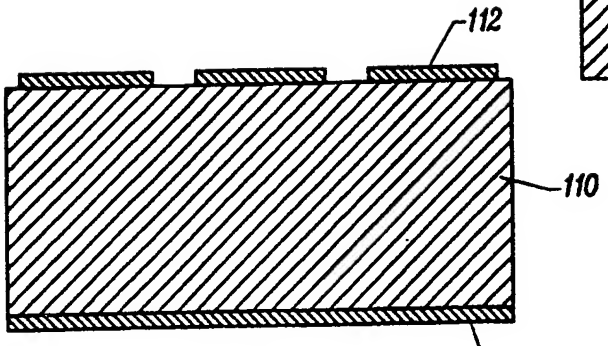

FIG. 26c

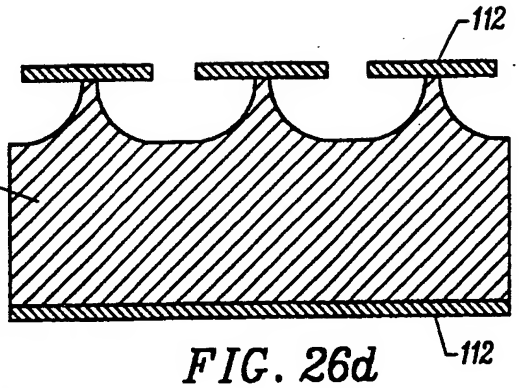

FIG. 26d

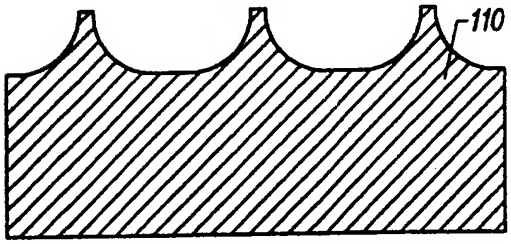

FIG. 26e

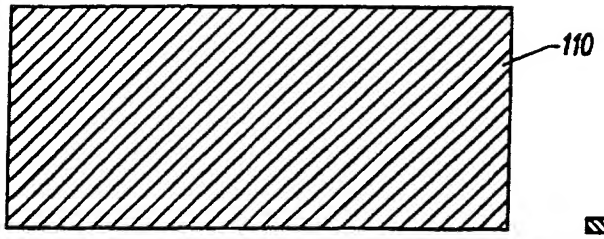

FIG. 27a

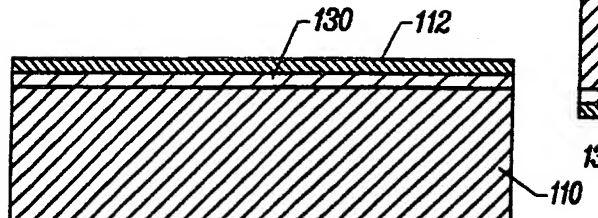

FIG. 27b

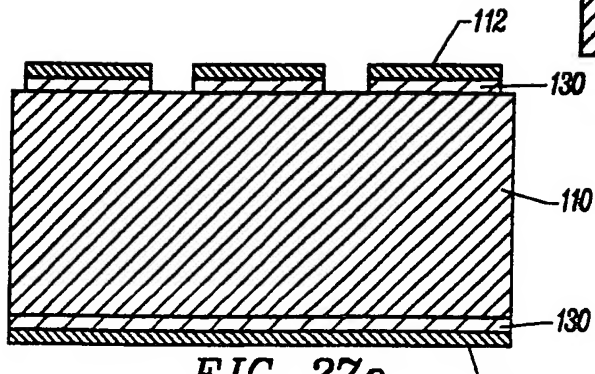

FIG. 27c

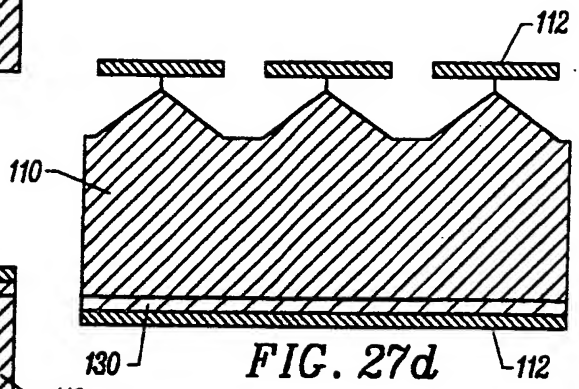

FIG. 27d

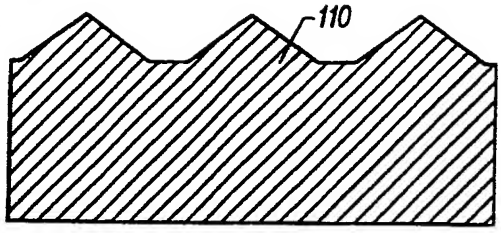

FIG. 27e

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US98/13560

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :A61M 5/32
US CL :604/272

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 604/264, 272-274; 606/222-224

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US, 5,342,397 A (GUIDO) 30 August 1994, cols. 1-8.	1, 11
Y	LIN, Lewei et al. Silicon Processed Microneedles, The 7th International Conference on Solid-State Sensors and Actuators, Transducers 1993 held in Kohama, Japan, June 7-10 1993, Department of Mechanical Engineering, University of California at Berkeley, California, pages 237-240.	2-9, 12-20

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search
31 JULY 1998

Date of mailing of the international search report
15 SEP 1998

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